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Curie point written magnetoresistive memory

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Memory cells have been fabricated and tested to demonstrate storage in the pinned layer of a giant magnetoresistance (GMR) spin valve film. The spin valve was top pinned with a FeMn film and gave about 4% GMR ratio. The memory cell consisted of an oblong, 0.6 μm×7.0 μm GMR bit with first metal contacts at each end and a perpendicular first and second metal word line passing over the bit. Joule heating due to current pulses through both the memory cell and the word line raised the temperature of the FeMn pinning layer above its Néel point. The magnetic field generated by the word line current switched the pinning direction, depending on the polarity of the word line current. Sense line currents up to 5 mA provided a half select without disturbing the bit. In combination with a 5 mA sense current, the bit was written with a word current pulse of 190 mA. The improved thermal stability of the pinned storage layer memory cell is shown to become necessary as the size of a magnetoresistive memory cell drops below about 0.1 μm×0.4 μm. © *2000 American Institute of Physics.* [S0021-8979(00)43808-9]

I. INTRODUCTION

Over the past few years, the scope of magnetoresistive random access memory (MRAM) research has expanded from a single material, a sandwich of two anisotropic magnetoresistive films, to a number of different giant magnetoresistance (GMR) materials, including tunneling materials, that use various memory storage, and readout methods. One common thread among these different types of MRAM is that they use an unpinned magnetic film for information storage.[1–4] The Curie point written (CPW) MRAM, using a spin valve (SV) material, is unique in that it uses a pinned magnetic film for information storage—which provides improved thermal stability, allowing further scaling to deep submicron cell dimensions, compared to other MRAMs.

To determine the point at which the ''traditional'' MRAMs hit thermal limitations, consider a memory with a 125 °C maximum temperature and a probability of a thermally induced loss of information of 10^{-5} for a year of continuous operation. This conservative value is about an order of magnitude less than the typical chance of device failure. Although thermally induced errors can be corrected with error correction circuitry, the error rate increases very rapidly with a reduction of the energy well depth. A reduction in well depth by 10 kT would increase the error rate by 22 026, while a reduction of 20 kT would increase the error rate to one per second.

Furthermore, assume that the memory architecture creates 500 half selected cells with fields applied $\frac{1}{3}$ of the time during a memory cycle. Also, the cells considered usually have one or two normal modes of oscillation with a decay time of 0.5–1.0 ns for the mode with the lower frequency. Thus, the required energy well depth for the lowest energy mode can be found from the expression

$$10^{-5}=2\times 10^{9}\times 3600\times 24\times 365\times 500\times 1/3\times e^{-(E_W/\mathrm{kT})}, \quad (1)$$

where E_W is the well depth for the mode, 2×10^9 is the inverse of the relaxation time, $3600\times 24\times 365$ is the number of seconds in a year, 500 is the number of half selected cells, and 1/3 is the fraction of time that the cells are half selected.[5]

From Eq. (1), it is seen that the necessary energy well depth is 55 kT. When half selected by a word field equal to 1/2 the anisotropy field, a magnetic memory cell with a Stoner–Wohlfarth threshold has its well depth reduced to 1/4 of the quiescent value of $1/2\times H_k\times M\times V$, where H_k is the anisotropy field, M is the saturation magnetization, and V is the volume. For a typical GMR magnetic film with a thickness of 15 Å, a 0.1 μm×0.4 μm memory bit has an energy well depth of about 55 kT. It is at this size, that a scaling limit is reached, because of thermal upset, for the unpinned storage films.

The pinned storage film in a CPW MRAM cell has a higher anisotropy than the unpinned films mentioned earlier. Thus, the energy well depth under half select conditions is greater, for a given bit volume, than that of the unpinned bit. This greater energy well allows the CPW bit to be scaled to smaller dimensions before thermal upset becomes a limiting factor in the cell's operation. The following sections present an initial demonstration of the CPW cell. It is shown that current pulses in the word and sense lines, as would be used in an array cross-point selection architecture, are sufficient to write the pinned film. Nondestructive readout of the stored state is accomplished by switching the soft layer of the CPW SV film.

II. EXPERIMENTAL PROCEDURE

The starting material for this experiment was a simple spin valve with the following layers and thicknesses:

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$$\mathrm{NiFe(70\ \AA)-Co(15\ \AA)-Cu(40\ \AA)-Co(15\ \AA)-NiFe(20\ \AA)-FeMn(125\ \AA)}.$$

The SV film was sputter deposited and had a modest GMR ratio of about 4%. The SV film was patterned, using an ion mill, into 0.6 μm×7 μm MRAM bits with tapered ends. An aluminum metal layer was deposited and patterned to connect the bits into five bit sense lines and to form word lines passing over the top of the bits. A second aluminum metal layer was used to provide a second turn over the bit for the word line.

These CPW bits are written by heating and cooling the bits in the presence of a magnetic field. For the write to be successful, the bit must reach a temperature above the Néel temperature of the FeMn pinning layer. Both the heating and the applied field must come from the sense line and word line. The first characterization step was to determine the magnitude of sense current that was required to write the bit. This was done by: (1) applying a fixed field to the bit in a direction opposite that of the pinning direction, (2) turning on a fixed sense current, (3) measuring the MR characteristic of the bit, and (4) repeating steps (1)–(3) with a larger sense current until a distinct reversal of the pinning orientation was seen.

Once the bit was characterized with respect to sense current, the word current requirements were determined. This was done by choosing a sense current magnitude that was just below the disturb level and then alternately decreasing the word current and measuring the MR characteristic of the bit. This second test determined the minimum word current that was required to write the bit when the maximum no-disturb sense current was applied.

III. RESULTS AND DISCUSSION

Figure 1 shows the MR traces that were obtained using an external field, applied parallel to the long axis of the bit, and varying sense currents through the CPW bits. Each of the three plots in Fig. 1 contain two traces, one for each polarity of the external field. The top, middle, and bottom plot shows the results that were obtained with a 4, 5, and 6 mA sense line current pulse, respectively. As can be seen in the top plot of Fig. 1, a 4 mA sense line current pulse does not heat the FeMn pinning layer sufficiently for the pinning direction to be reversed. At 5 mA, there is an increase in the high field hysteresis, but the overall pinning orientation appears undisturbed. As shown in the bottom plot of Fig. 1, a 6 mA pulse provides sufficient heating to cause a significant change in the FeMn pinning.

From these data, it is determined that 5 mA is the maximum acceptable sense line current for a 2D array select. This level of sense line current, a half select current, will not, by itself, disturb the bits on a sense line. Next, it must be shown that this current, in conjunction with a word line current, is sufficient to write the bit. Figure 2 shows the MR traces that resulted when a CPW bit was simultaneously subjected to a 5 mA sense line current and a word line current of 170–220 mA. In each of the six plots shown in Fig. 2, there are two traces—one obtained following a positive word current pulse and one obtained following a negative word current pulse. While either polarity of word current should produce the same amount of bit heating, the polarity of the word line current determines the direction of the word line generated magnetic field with respect to the long axis of the CPW bit.

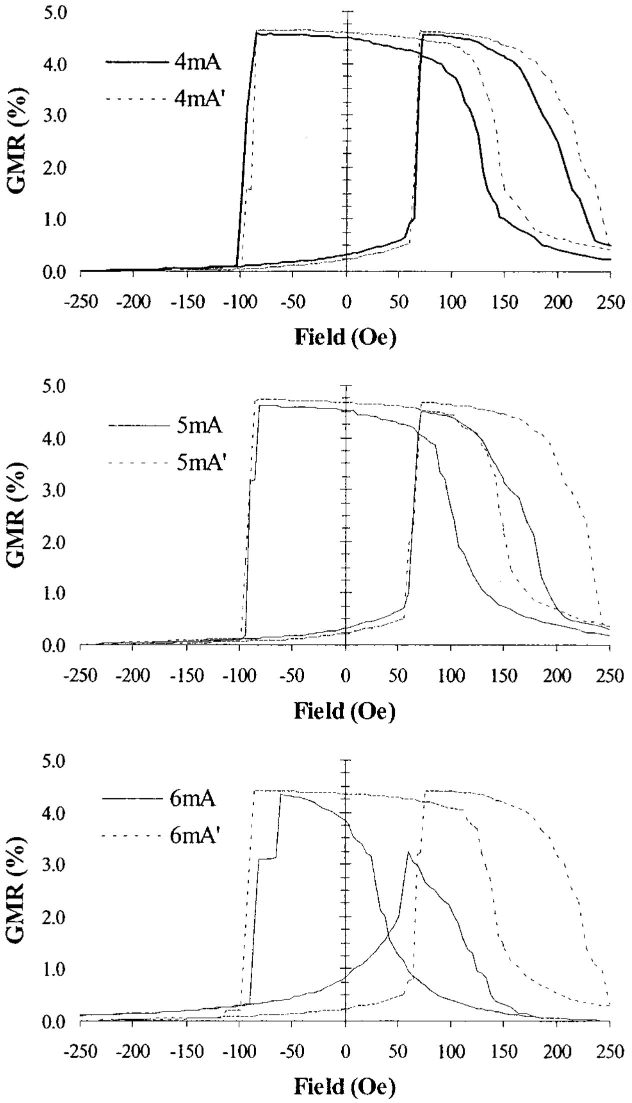

FIG. 1. MR traces obtained from a CPW bit following application of 4, 5, and 6 mA sense current pulses. The polarity of an external field, applied parallel to the long axis of the bit, was changed between the solid and dashed traces. A 1 mA sense current was used to obtain the MR traces.

At the highest current level, 220 mA, the mirroring of the MR trace between application of first a positive and then a negative word line current pulse clearly indicates that the combination of sense line and word line pulses has been sufficient to reverse the pinning direction of the FeMn film. This demonstrates the basic CPW concept—that selfheating from sense line and word line current, along with the field generated by the word line current, is sufficient to reorient the FeMn pinning. As the magnitude of the word line current pulse is decreased, the quality of the pinning reversal decreases. From the lower right plot of Fig. 2, with a 170 mW word current pulse, the pinning has clearly not been adequately reversed. At a current level of 190–200 mA the reversal still appears to be reasonably complete.

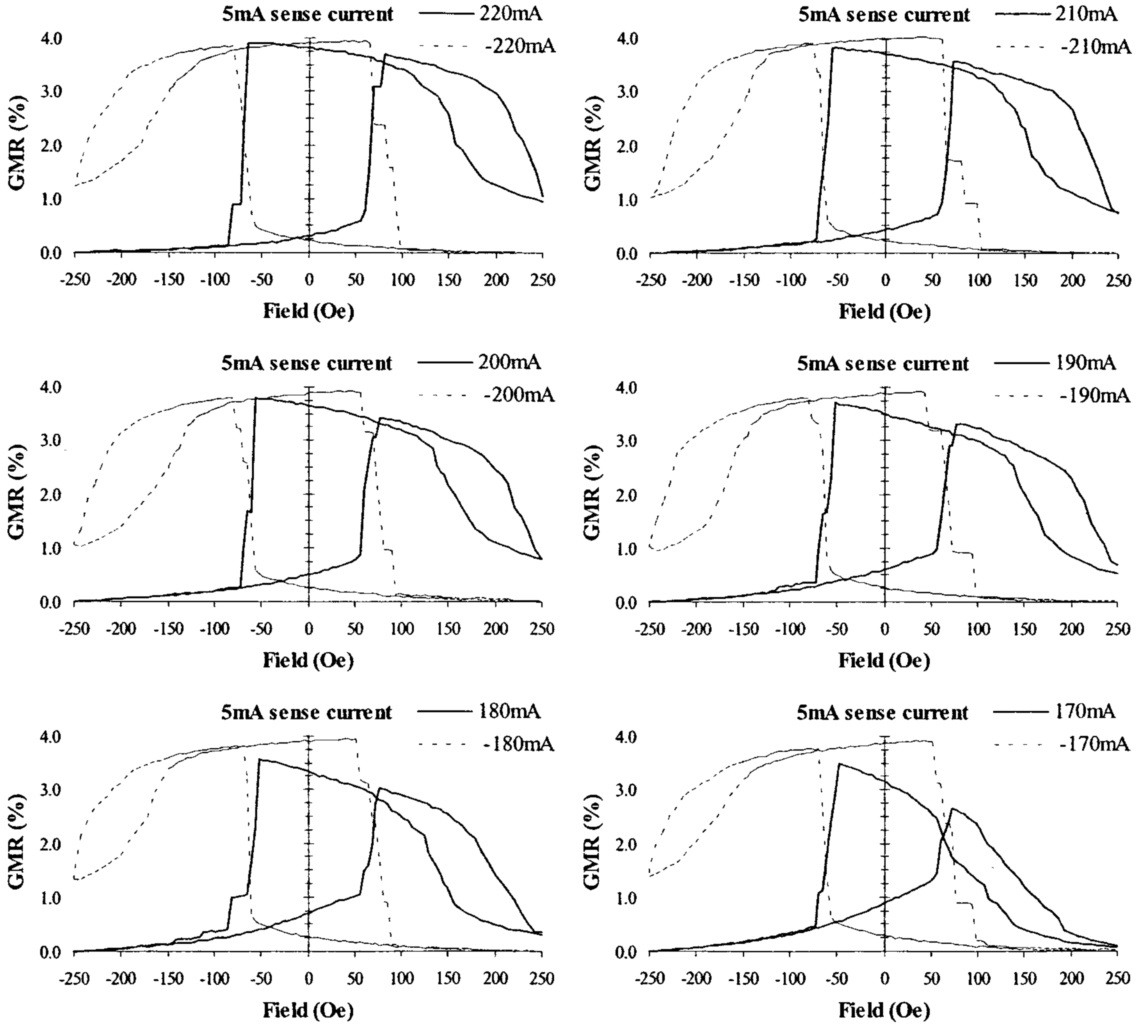

FIG. 2. MR traces obtained from a CPW bit following simultaneous application of sense and word current pulses. A fixed 5 mA sense current pulse was used, while the word current pulse varied in magnitude from 170 to 220 mA. The two traces in each plot correspond to opposite polarities of the word current pulse. A 1 mA sense current was used to obtain the MR traces.

IV. CONCLUSIONS

The work presented clearly shows the feasibility of the CPW MRAM concept. Application of both sense and word currents is sufficient to reorient the FeMn pinning layer and write the bit, while one of these currents acting alone does not write the bit. Future work will concentrate on improving the thermal design of the CPW cell so that the current levels required to write the bit can be significantly decreased. Relative to this quick proof-of-concept experiment, decreased word line thermal mass, decreased insulator thickness, and increased word line resistance over the bit are all obvious areas of potential improvement in the cell's thermal design.

ACKNOWLEDGMENT

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