

Address line-assisted switching of vertical magnetoresistive random access memory (VMRAM) cells

John M. Anderson and David J. Brownell
NVE Corporation

Gary A. Prinz, Harold Huggins, Luan V. Van, and
Joseph A. Christodoulides
Naval Research Laboratory

Jian-Gang Zhu
Carnegie-Mellon University



Presentation Outline

- VMRAM Overview
- VMRAM Technology
 - Bits and Sense Lines
 - MR Response
 - Reading and Writing
 - Arrays w/ Address Lines
- Test and Analysis
- IC Prototype
- VMRAM vs. Hard Disk Drive
- Conclusion

VMRAM Overview

- VMRAM = Vertical Magnetoresistive Random Access Memory
- Devised and developed by researchers at NRL and CMU
 - NRL: Dr. Gary Prinz^{1,2,3}, Dr. Konrad Bussmann²
 - CMU: Dr. Jian-Gang Zhu¹
- VMRAM cells consist of toroid-shaped elements that have a stable closed-flux magnetic configuration
- Employs current perpendicular to the plane (CPP) to switch soft (read) and hard (write) magnetic layers of a GMR multilayer
- Address (word) lines generate radial torque fields that assist switching
- Teams from NVE Corp. and NRL have developed processes to fabricate 64-bit strings of 0.6 μm O.D./0.2 μm I.D. cells with address lines
- VMRAM is a high-density, non-volatile memory theoretically scaleable to 400Gbits/in² at $\lambda = 10\text{nm}$ ¹ and has the potential to compete with both semiconductor memories and mechanical hard disks.

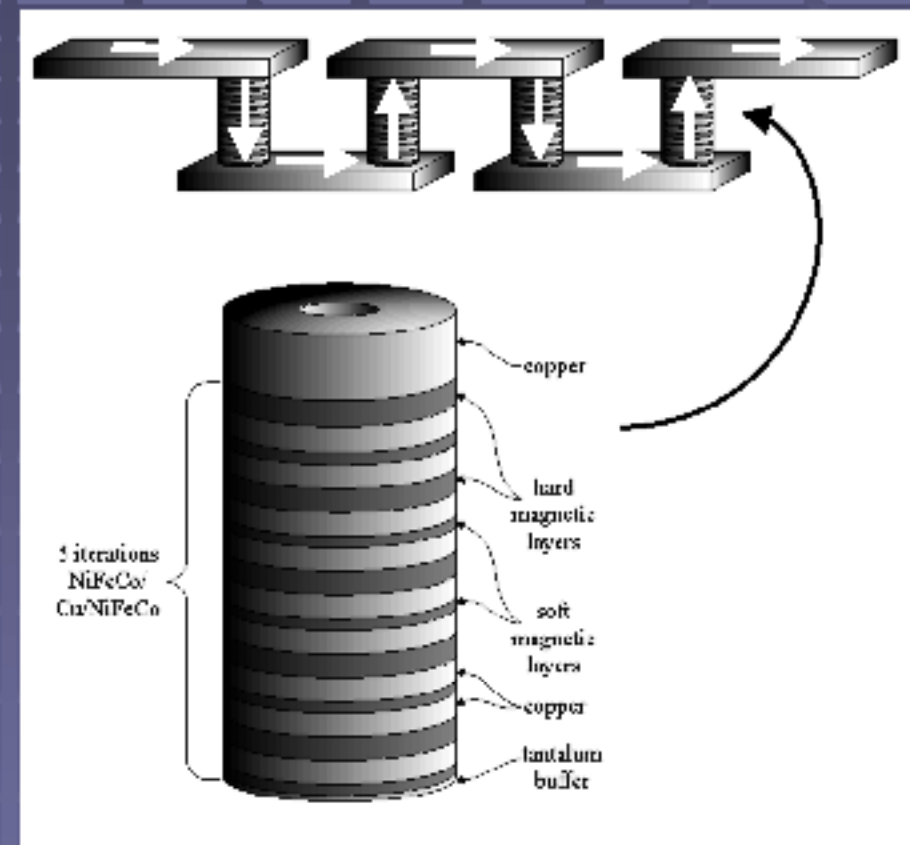
¹J.-G. Zhu, Y. Zheng, and G.A. Prinz, J. Appl. Phys. **87**, 6668 (2000).

²K. Bussman, G.A. Prinz, R. Bass, J.-G. Zhu, Appl. Phys. Ltrs. **78**, 2029 (2001).

³G. Prinz, U.S. Patent No. 5477482

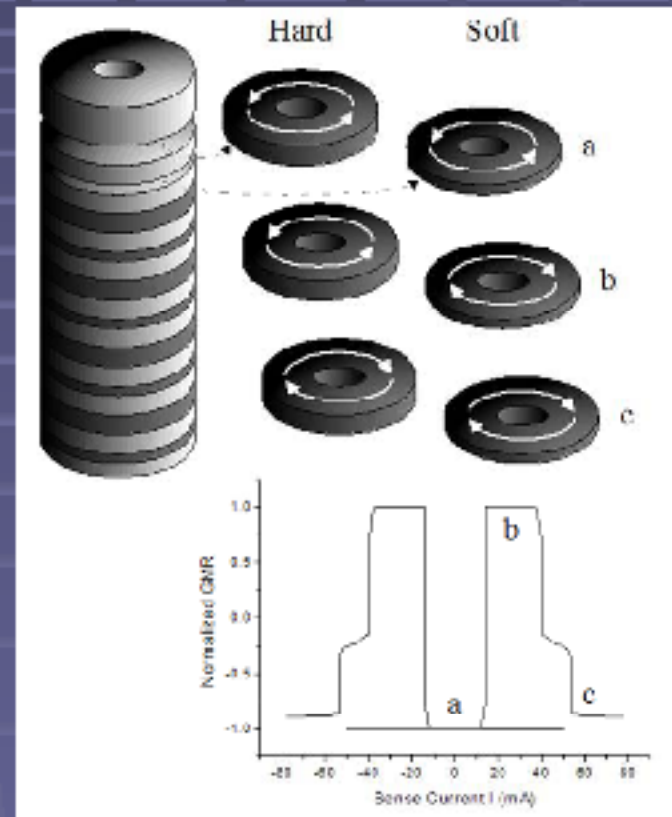
VMRAM Technology – Bits and Sense Lines

- 2000Å CMP'd Cu
- 40Å Ta phase breaking layer
- Multilayer stacks:
[NiFeCo (20Å)/Cu (40Å)/
NiFeCo (40Å)/Cu (40Å)]x5
- 2000Å Cu connects cells such that current flows vertically
- Test arrays consist of 256 bits in 4x64-bit strings

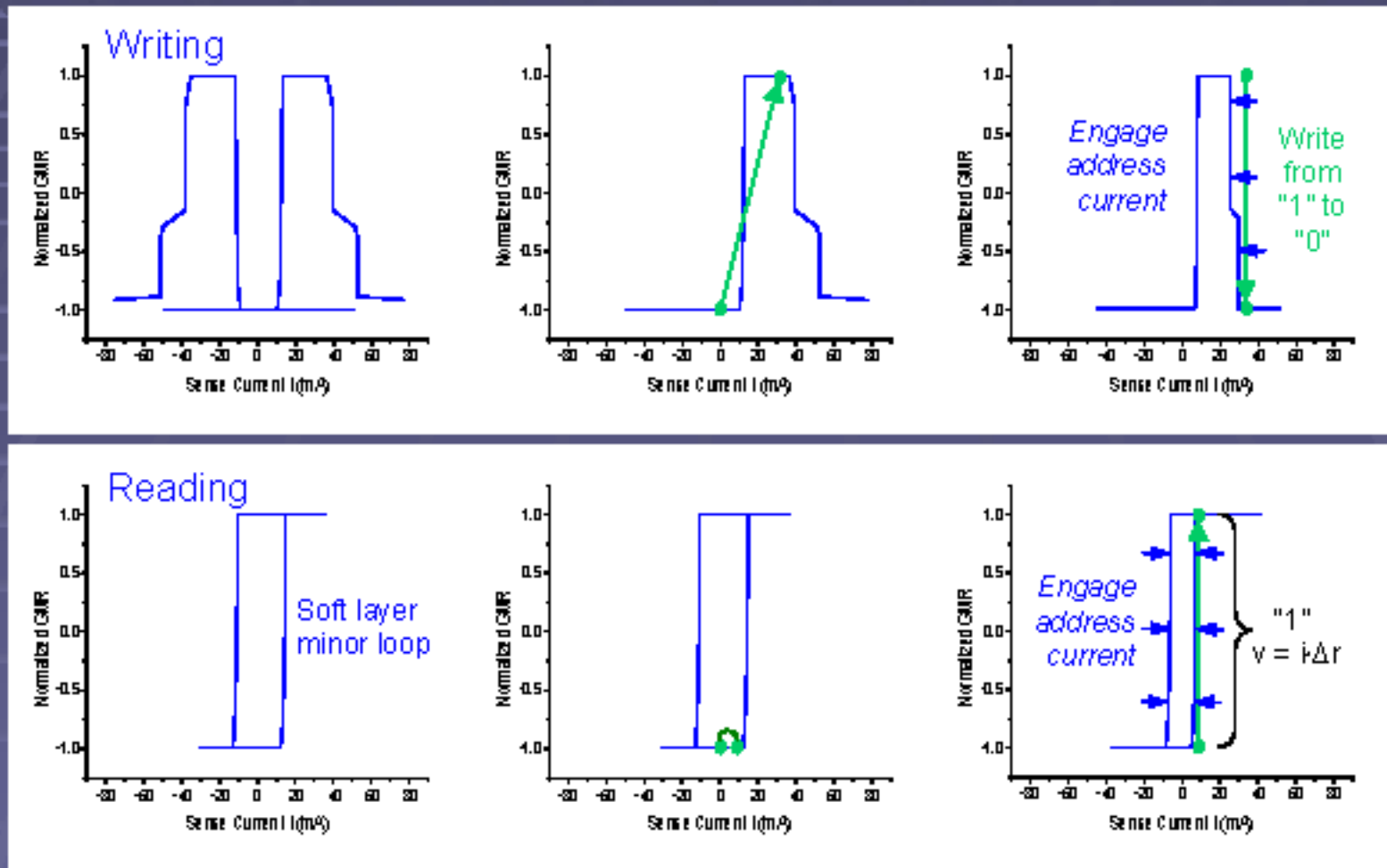


VMRAM Technology – MR Response

- Response shape is similar to pseudo-spin valve
- Thicker (hard) layers act as storage mechanisms
- Thinner (soft) layers act as read mechanisms
- Simulated Response
 - Soft layers switch ~15mA
 - Hard layers switch 40 – 55mA
- Address line current effectively reduces switch thresholds

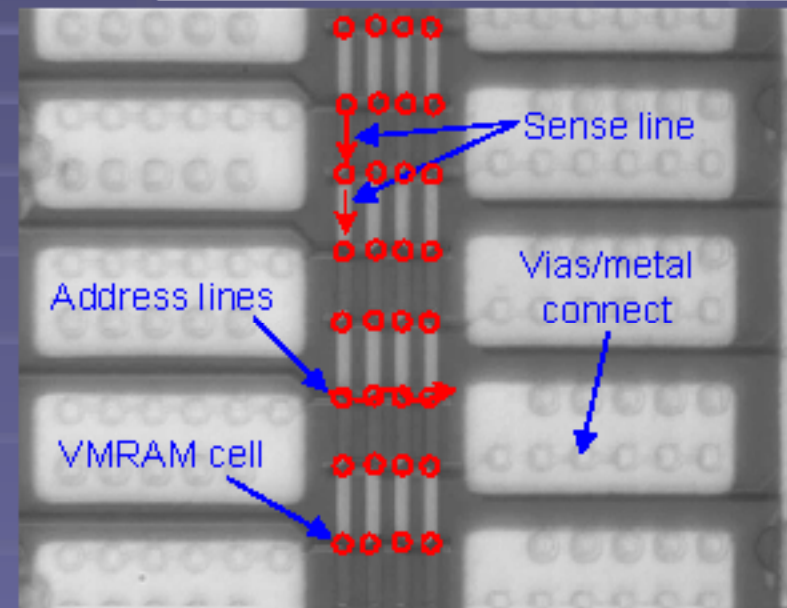
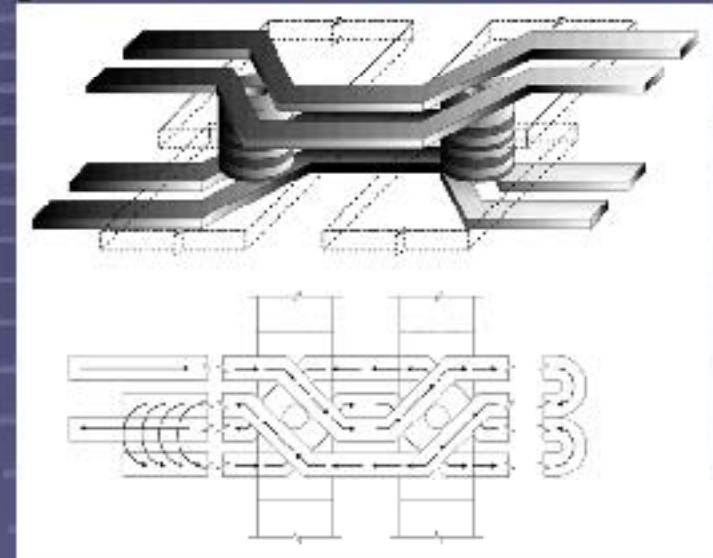


VMRAM Technology – Writing/Reading



VMRAM Technology – Array w/ Address Lines

- Serpentine arrangement yields orthogonal upper/lower address lines
- Address current generates an outward radial word field for the current direction shown
- 4x64 arrays (4x8 section shown)
 - 4 sense lines run vertically
 - Address lines run horizontally
- 2-D selection
- Top and bottom address line segments connect through vias
- VMRAM cells reside at the junctions – 32 cells shown



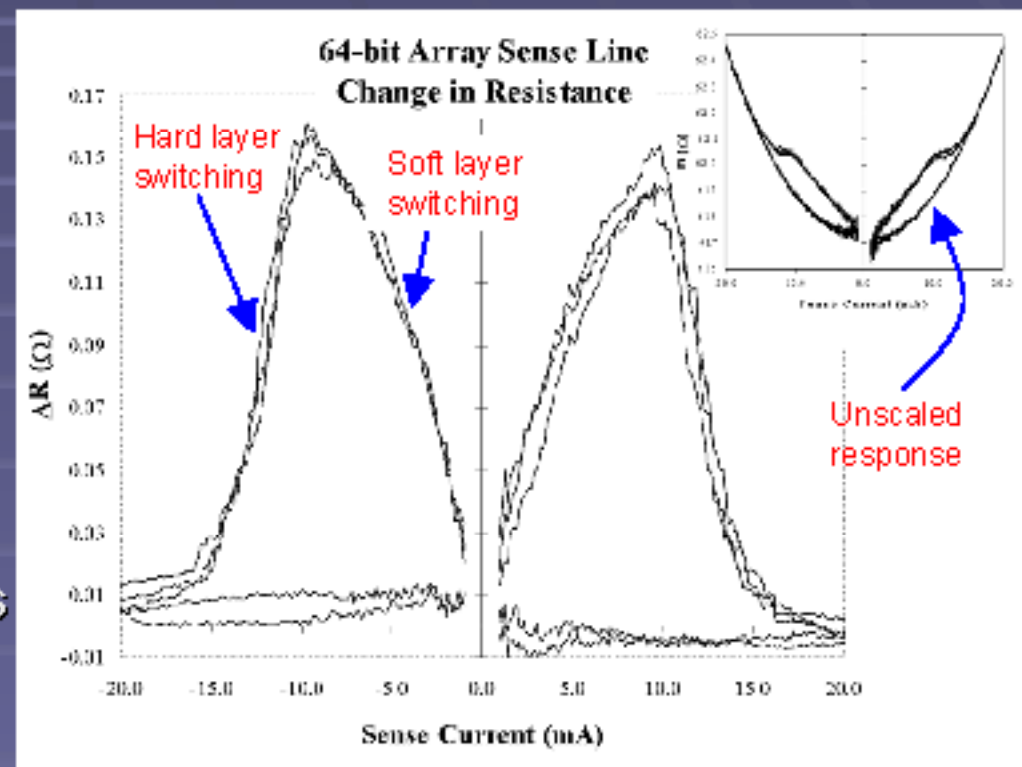
Test and Analysis – General Test Procedure

- Run bipolar sense current sweep to determine switch thresholds ($\pm I_{th}$)
- Establish reference by saturating bits with $+I_{th}$ mA and sweeping the sense line with the same polarity current
- Saturate sense line with $< |-I_{th}|$ mA and I_{addr} mA
- Sweep sense current from $+I_{small}$ mA to $+I_{th}$ mA
- Read voltage at each sense current step:
 - Sample voltage
 - Assert address current
 - Sample voltage
- Generate MR transfer curve
- Scale data by subtracting out reference curve

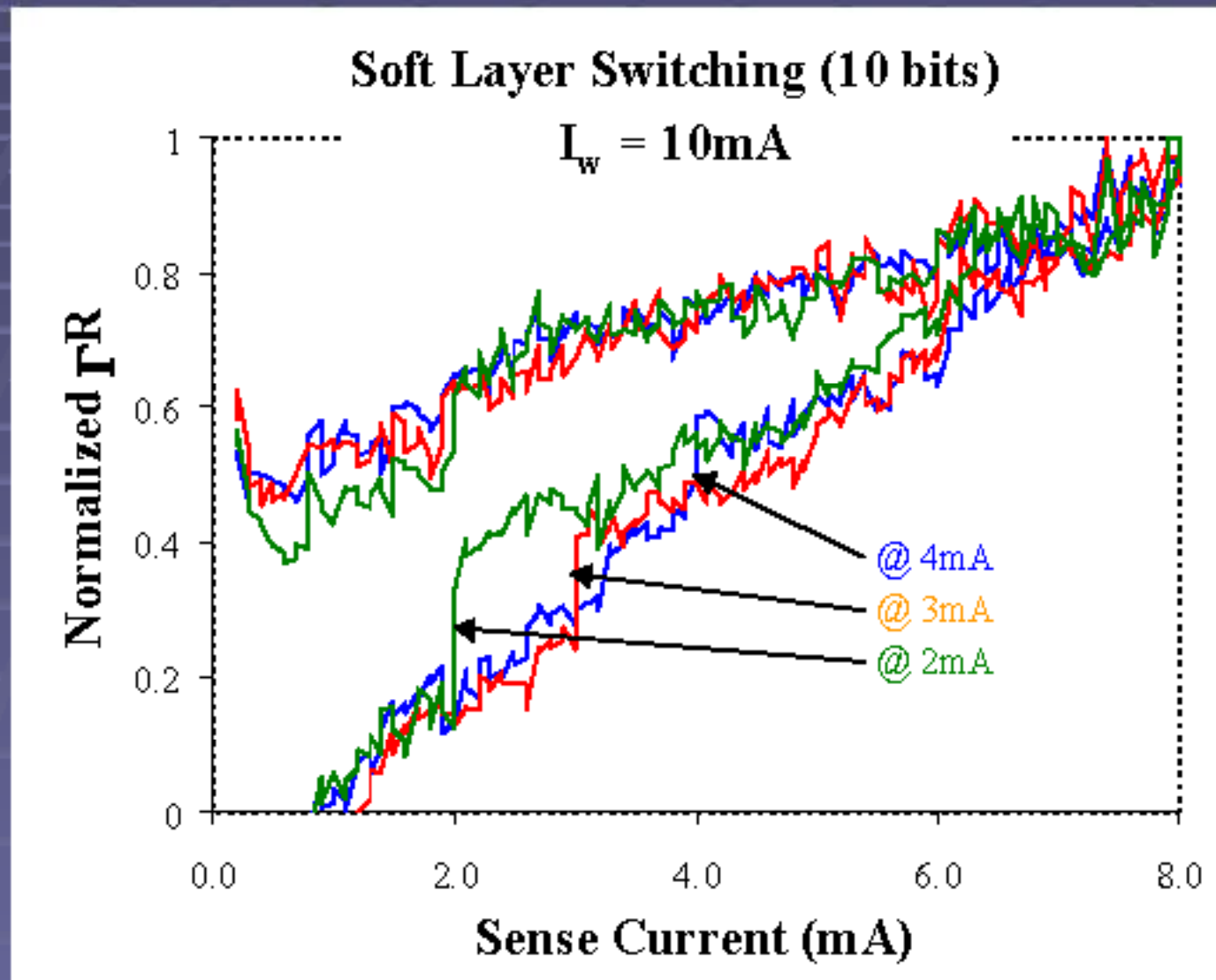
Test and Analysis – MR Response

- Observations:
 - GMR <1% vs. 10%-20%
 - Smooth transitions for hard and soft layers vs. abrupt switching

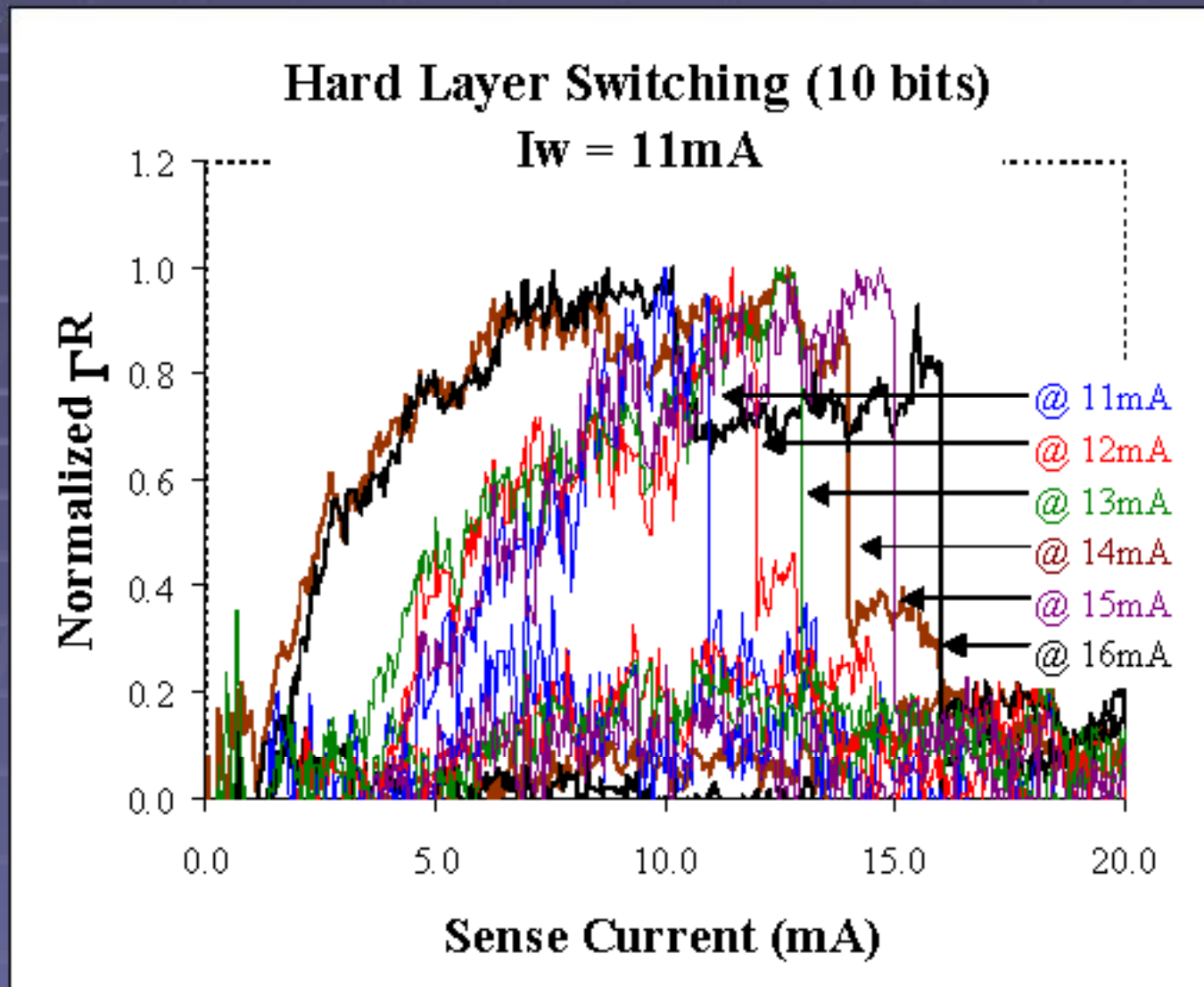
- Suspected cause: magnetic material redeposition
 - couples the stack layers
 - limits antiparallel alignment between hard/soft layers
 - and/or, significantly reduces the number of “active” layers



Test and Analysis – Read Layer



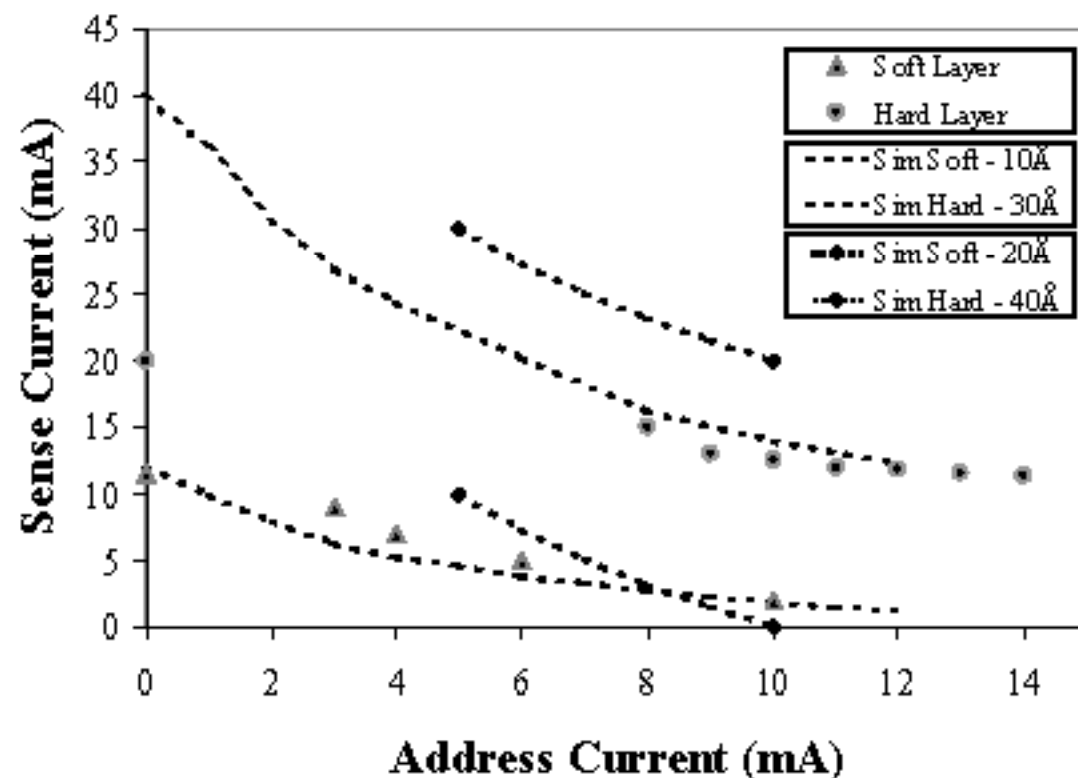
Test and Analysis – Write Layer



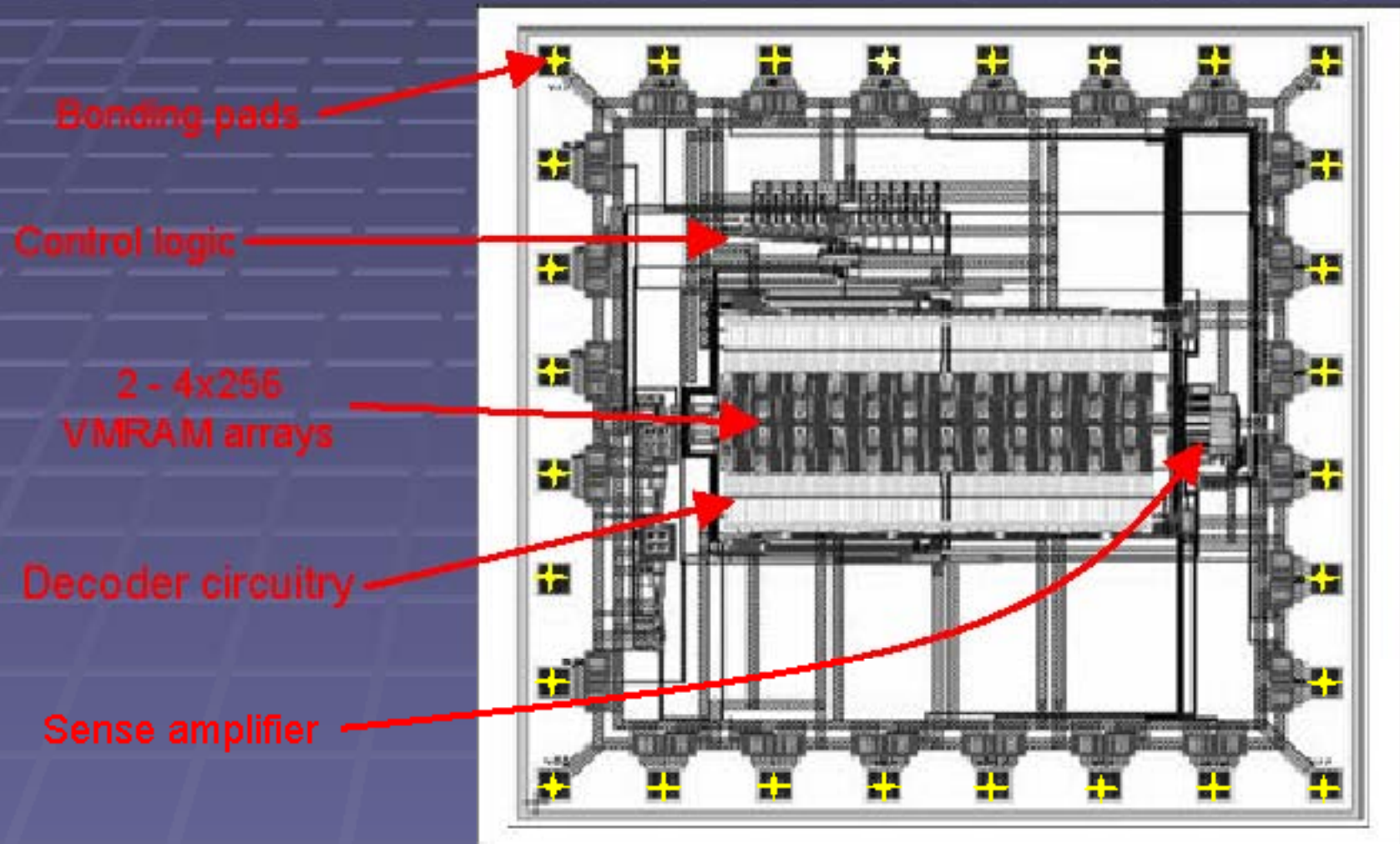
Test and Analysis – Switching Asteroid

- Soft layer operating point
 - $I_{\text{sense}} = 6\text{mA}$
 - $I_{\text{addr.}} = 5\text{mA}$
- Hard layer operating point
 - $I_{\text{sense}} = 12\text{mA}$
 - $I_{\text{addr.}} = 10\text{mA}$
- Experimental data tends toward simulated 10Å/30Å combination

**VMRAM Switching Asteroid
Experimental vs. Simulated**



VMRAM 2K IC Prototype Design



VMRAM vs. HDD (Projected)

- VMRAM Density at $\lambda = 0.01\mu\text{m}$ node
 - Best case: $16\lambda^2 = 403 \text{ Gbits/in}^2$
 - Worst case: $18.77\lambda^2 = 358 \text{ Gbits/in}^2$
- VMRAM compared to a 147GB HDD*
 - $\lambda = 0.09\mu\text{m}$ node
 - 9mm x 9mm PLCC package can hold 270 – 305Mb
 - HDD* FF $\Rightarrow 4" \times 5.78" \times 1.03"$
 - Same sized VMRAM memory module yields 65 – 75GB
 - *A VMRAM memory module built today could have ~50% the capacity of today's HDD*
 - *At $\lambda = 0.08\mu\text{m}$ (ITRS projection for 2005) capacity is ~65%*
- VMRAM has no mechanical wearout
- Smaller, rugged, more versatile form factor

*Maxtor Atlas[®] 15K II

Conclusion

- Four by sixty-four bit VMRAM test arrays were successfully fabricated using address lines designed for 2-D selection.
- Address-assisted switching of VMRAM cells was demonstrated
 - Soft layer switching: $I_{\text{sense}} = 6\text{mA}$, $I_{\text{addr.}} = 5\text{mA}$
 - Hard layer switching: $I_{\text{sense}} = 12\text{mA}$, $I_{\text{addr.}} = 10\text{mA}$
- Edge pinning in the GMR stack due to magnetic material redeposition led to low signal response and smooth transitions in unassisted MR response.
- GMR multilayer optimization is needed in order to maximize signal and ensure “singular” switching thresholds for stack magnetic layers.
- Integrated 2K VMRAM prototype design has been completed for a $0.35\mu\text{m}$ gate length semiconductor process.
- Hard and soft layer switching asteroids generated from experimental data compare well with micromagnetic simulations.
- ★ NVE Corporation thanks the Office of Naval Research and the Naval Research Laboratory for their continued support and collaboration