

Low Power 256K MRAM Design

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Abstract—A low power Magnetoresistive Random Access Memory (MRAM), that uses a novel Sandwich-Spin Dependent Tunneling (SSDT) memory bit is described. The SSDT bit combines a sandwich storage structure with tunneling magnetoresistance readout. A single, bi-polar write current is used to write the bit. A write select transistor, in the memory cell, selects a single bit for writing - thereby eliminating half-select conditions. Antiferromagnetic coupling in the sandwich film minimizes the required switching field, leading to low write currents - as low as 4 mA seen in 2 μm devices and 0.8 mA predicted for an 0.6 μm device. A two bit, differential cell, has been used to design a 256k memory.

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1. INTRODUCTION

MRAM has been under development for roughly 15 years. During that time, the magnetoresistive technology that has been used in the design concepts has included Anisotropic Magneto-Resistance (AMR), Giant Magneto-Resistance (GMR), Spin Valve (SV), Pseudo Spin Valve (PSV), and Spin Dependent Tunneling (SDT, sometimes referred to as Magnetic Tunnel Junction, or MTJ). Along with these different MR materials, the MRAM concepts have used a variety of cell architectures and operating modes. Despite this long development and variety of magnetoresistive technologies, a commercial MRAM still has not been developed and produced. Two of the primary reasons for this lack of a commercial MRAM are: 1) high write current requirement, and 2) lack of bit uniformity. These two problems affect both yield and reliability, as well as practicality or commercial feasibility. The SSDT cell addresses both of these problems by having a significantly lower write current

than previous MRAM concepts, and by eliminating the half-select situation that puts severe constraints on the bit uniformity in previous MRAMs.

2. POWER AND UNIFORMITY PROBLEMS

High write current requirements put limitations on the cell and memory size and affect the reliability of the memory. From a current steering standpoint, as needed to direct the write currents to the appropriate cell, relatively large transistors are required in order to handle the high write current. Compared to a traditional memory, these write transistors take up a disproportionate fraction of the die size and lead to a larger die. In array layout, the size of these write transistors can limit the pitch of the rows and/or columns. High write currents also require wider metal lines, in order to avoid electromigration, and multiple contacts and/or vias, to connect between metal layers or from a metal layer to an active device. These wide metal lines limit the density of the memory. Also, narrower lines and single contacts are generally required in order to make the connection to the bit - leading to a situation in which the electromigration limit is easily exceeded. Finally, the overall memory current, when a byte wide, or larger, write operation is required, can become quite large if the write current for a single cell is large. This total chip current, compared to traditional memories, can make the memory unattractive, especially in low power and battery operated applications.

Issues with cell uniformity generally stem from the cell design and mode of operation. The typical SDT based MRAM cell uses 2-D magnetic selection for the write operation. Figures 1 and 2, that show the read and write modes for a popular SDT cell, help to illustrate how this works. For the read mode, as shown in Fig. 1, there is no magnetic selection. Instead, a pass transistor selects a single cell, from a column or row, depending on the memory architecture, to connect to the bit line and receive the sense current. A voltage is developed across the cell, in response to the sense current, and is detected by the readout circuitry. Generally, the cell voltage is compared to a fixed reference voltage in order to determine the state of the cell. Because the cell does not depend upon current-generated magnetic fields for the read mode, the read mode is not a source of uniformity problems.

3. SSDT CELL

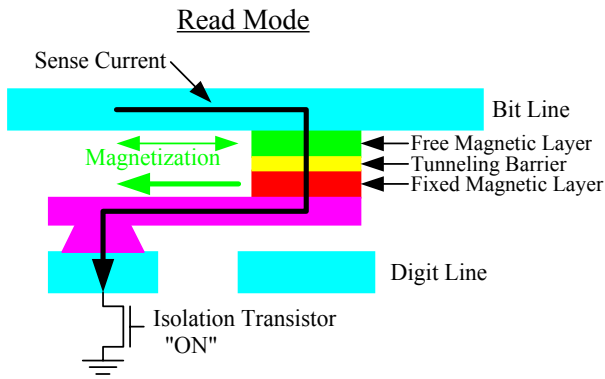


Figure 1. Read mode of a popular SDT cell design. A transistor is used to select a single SDT bit for the read operation.

In the write mode of this SDT cell, shown in Fig. 2, two current conductors, the bit line and the digit line, each carry a write current past the SDT bit. The free magnetic layer of the SDT bit, in close proximity to these current carrying conductors, is switched by the magnetic fields that the currents generate. Taking the bit line to be a 'row' conductor in the memory array, it is clear that all bits in the selected row will experience the field that is generated by the bit line current. Similarly, each bit in a selected column will be exposed to the field that is generated by the digit line current. These 'half-select' fields can disturb un-selected bits on a row or column.

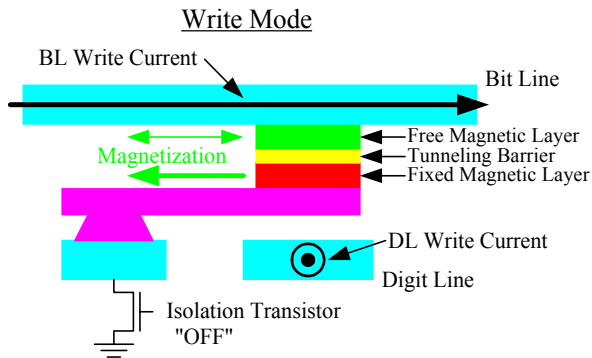


Figure 2. Write mode of a popular SDT cell design. The bit at the cross-point of the digit line and bit line is written by the fields that they generate.

In order to ensure that every bit can be written, the bit line and digit line currents must be set high enough so that they write the bit that has the highest switching threshold. If the range of switching thresholds is large, due to poor bit uniformity, then this can lead to disturbs of the bits that have low switching thresholds. Achieving suitable uniformity between bits, so that disturbs do not occur, has been an elusive goal. Because the switching threshold is affected by subtle changes in material properties and bit shape, it is hard to control the threshold and make it uniform.

The SSDT memory cell addresses the issues of high power and half-select disturbs through a unique bit structure and the use of a second select transistor in the memory cell. The antiferromagnetically coupled sandwich film that is used as the storage (free) layer in the SSDT bit requires significantly less current to switch than is required in the popular cell that is shown in Figs. 1 and 2. This structure is also immune to disturbs by the external fields that are generated by on-chip current conductors. Also, with only a single write current, that is selectively passed through only a single cell, half-select conditions are eliminated.

In a traditional, single free layer, SDT bit, the switching magnetization is uncompensated. Consider the switching sequence that is illustrated in Fig. 3. In response to external magnetic fields, the magnetization rotates to being parallel with the narrow dimension of the bit and a high demagnetization field is created - tending to resist the rotation, or switching, of the film. Relatively large fields are required to overcome this high energy state and switch the bit. This requires large write currents.

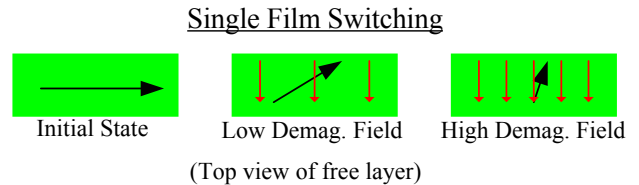


Figure 3. Top view of a single layer free film during switching. High demagnetization field occurs as magnetization swings through short axis of the bit.

The sandwich free layer in the SSDT bit contains two magnetic layers that are separated by a non-magnetic layer. If the non-magnetic layer is a thin ruthenium film, then the magnetic layers will be strongly antiferromagnetically coupled. Because of this strong coupling, the two magnetic films will remain anti-parallel, even during switching. Thus, the demagnetization field that is generated by one layer is compensated by an opposite demagnetization layer that is generated by the other layer. As shown in Fig. 4, only a very minimal net demagnetization field is created, for each layer, as the magnetizations of the pair of films rotates to being parallel with the short axis of the bit. Only a small field is required to overcome this lower energy rotation state - so a smaller current is able to switch this sandwich film. Empirical data shows that only a 4 mA write current in a 2 μm wide device is required for switching. This data agrees with a theoretical model, that predicts that an 0.6 μm wide device will switch with a 0.8 mA write current.

Sandwich Film Switching

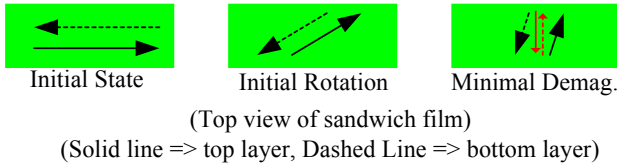


Figure 4. Top view of sandwich film during switching. Only minimal demagnetization fields are generated.

Because of the antiferromagnetic coupling in the sandwich film, keeping the magnetizations of the two layers antiparallel to each other, the magnetic state of the sandwich is not sensitive to external fields. Thus, the SSDT memory is immune to external fields as would normally be encountered in use - eliminating the need for magnetic shielding. Since external fields don't affect the sandwich, the SSDT bit is written by passing a current through the sandwich film. This current generates fields that are in opposite directions on the top and bottom magnetic layers. It is these relatively small, internally generated magnetic fields that switch the bit between its two memory states.

With a single write current, that must pass through one of the SSDT layers, the SSDT cell is significantly different from the popular SDT cell that was shown in Figs. 1 and 2. One notable difference is the absence of the digit line - the second, orthogonal write current is not needed in the SSDT cell. The other key difference is the inclusion of a second select transistor, that is used to steer the write current through the SSDT bit. These difference are illustrated in Fig. 5, which shows the write mode of the SSDT cell.

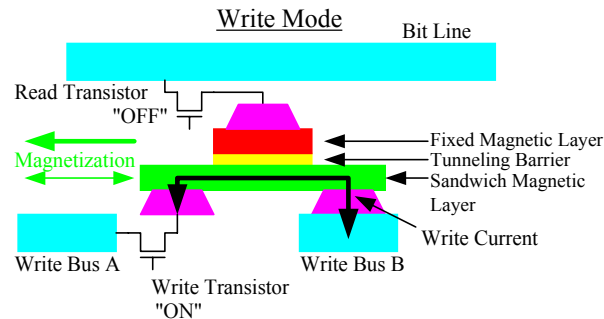


Figure 5. SSDT cell during write mode. Write current passes through the sandwich layer of the cell when the write transistor is on.

As shown in Fig. 5, only a single write current is used with the SSDT cell. Compared to the typical SDT cell, this cuts the write current in half - leading to a lower power memory. While the bus lines that carry the write current from the driver circuitry to the cell pass by a number of different cells, the write current only passes through the one cell whose select transistor is turned on. Thus, there are no half-select or disturb conditions on

other, non-selected cells in the array. Since the half-select condition has been eliminated, concerns with switching uniformity are also eliminated. Using a higher current than the minimum that is required for switching does not cause any problem. Thus, as long as the highest switching threshold in the array is within the limits of the write current drivers, all of the cells can be written without concern for the uniformity of the switching thresholds.

As shown in Fig. 6, the read configuration of the SSDT cell is also different from that of the SDT cell. One difference is that the read select transistor is at the "top" of the cell - connecting the SSDT bit to the bit line. With this arrangement, the read current does not return to ground within the cell. Instead, one, or both, of the write bus lines must provide the return path, or ground connection, for the read current. As with the SDT cell, once the read current is established in the SSDT cell, the cell voltage is sensed in order to determine the data state of the cell.

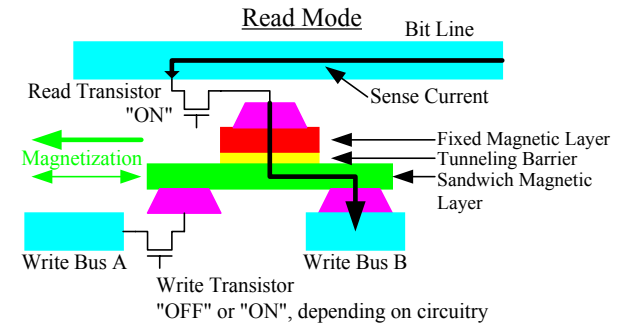


Figure 6. Read mode of the SSDT cell. Depending on the drive and select circuitry, the write transistor may be 'OFF' or 'ON' - to ground the sandwich layer.

4. 256K MEMORY

In light of the problems that have been seen, to date, in the development of MRAM, the goal of this memory design effort was to create a memory design that avoided the magnetic cell uniformity constraints and high power requirement of the typical MRAM design - resulting in a manufacturable device. The sandwich storage layer in the SSDT bit lowers the write current requirement, through closed flux switching, provides immunity to external disturb fields, and, in combination with a write current select transistor in the cell, eliminates half-select conditions that put tight uniformity restrictions on the magnetic characteristics of the bits. Thus, an MRAM that uses the SSDT bit should consume relatively low power and have high yield.

A common MRAM architecture uses a single bit-per-cell for data storage. During readout, the bit voltage is compared to a fixed reference voltage. This scheme

places additional constraints on the uniformity, in this case electrical uniformity, of the bits. If the resistances of the bits vary too much, then the margins between the bit's two states and the reference voltage can become too slim for reliable operation. Also, for optimum sensing, the reference voltage must be set to a point that is about midway between the high and low states of the bit. This cuts the sense signal in half with respect to the voltage difference between the bit's high and low states - this lower signal requires longer sense times, and therefore slower memory cycle time, in order to maintain a given signal-to-noise ratio in the sense circuit. Because of these issues, the single bit-per-cell architecture was rejected for the 256k design.

A two-bit-per-cell, differential read-out architecture was chosen for this effort. While this architecture yields a lower density array than the single-bit-per-cell architecture, the higher signal and local self-referencing provide a faster, more robust memory - which fit the overall goal of the design. Figure 7 shows a schematic of the two-bit cell. For writing, the write select transistor passes a single write current through both bits in the cell. In the cell layout, the bits are connected so that the current passes through the two bits in opposite directions - writing the two bits to opposite states. During readout, the two read select transistors are turned on, connecting the two bits to the two bit lines. The two bits, being written to opposite states, generate different voltages. This differential voltage is sensed in order to generate the logic cell output. This differential read scheme is very similar to a traditional SRAM, where the opposite sides of a flip-flop latch are connected to the bit lines.

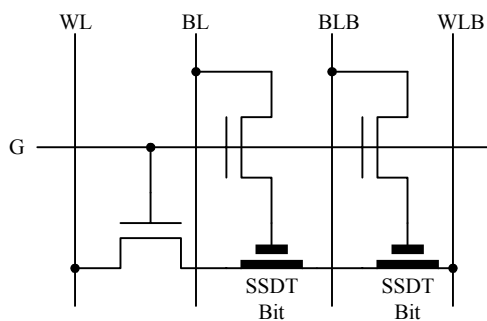


Figure 7. Schematic of a differential SSDT cell. A single gate line controls both write and read select transistors - both WL and WLB will be grounded during a read.

In the cell that is shown in Fig.7, a single gate line is used to turn on both the write select transistor and the read select transistors. With this configuration, both the WL and WLB lines must be grounded during a read operation. The WL and WLB lines are connected, at the periphery of the array, to the write drivers. The write drivers provide a bi-directional current, to write a '1' or '0', during a write cycle. Otherwise, they provide a ground connection for the read cycle. A layout for this differential SSDT cell is

shown in Fig. 8. This layout was designed to have the same pitch, on both x and y axes, as the memory cell of a commercial SRAM - so the SRAM could be used as a starting point for the MRAM design and layout.

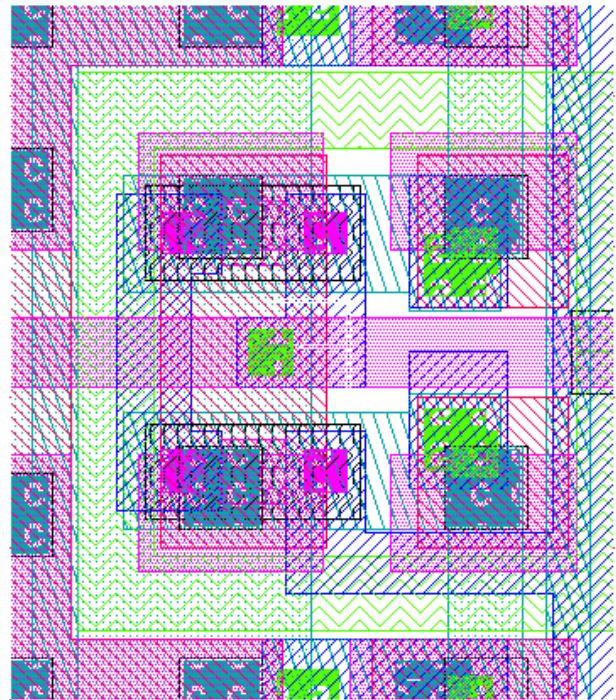


Figure 8. Layout of a differential SSDT cell. Two SSDT bits and two select transistors are contained in the same area as a commercial SRAM cell.

The SSDT cell layout is designed to be used in a 4-cell cluster. The features that are around the cell periphery and that have one or two axes of symmetry, i.e. contacts, metal lines, etc., are not completely contained in the cell layout. Instead, only 1/2 or 1/4 of a given feature is included in the cell. For example, only half the required width of a metal line, that runs along the cell edge, will be included in the cell layout. Then, when the cell is mirrored across the x-axis, the y-axis, and both axes, and the four cells are then butted up to one another, the periphery features are completed. This 4-cell cluster is then arrayed in order to form the full memory array. In this cluster, adjacent cells along a row will share one of the word lines. A schematic of the 4-cell cluster is shown in Fig. 9. Note that WLB is shared between the two cells along a row within the cluster. WL will be shared between clusters as they are placed along a row in order to create a bigger array.

Using the cell layout that is shown in Fig. 8, a 256k MRAM design has been completed. This design is based on an existing 256k SRAM design, and maintains the dies size and pad-out of the SRAM device. The SSDT bit has a width of 0.6 μm , which is expected to write with about 0.8 mA of current. This write current is an order of

magnitude lower than that of other SDT based MRAM designs. And, as described earlier, the SSDT cell is expected to give a significant boost to yield and manufacturability because of the elimination of the half-select condition and the resultant uniformity constraints on the magnetic and electrical characteristics of the bit.

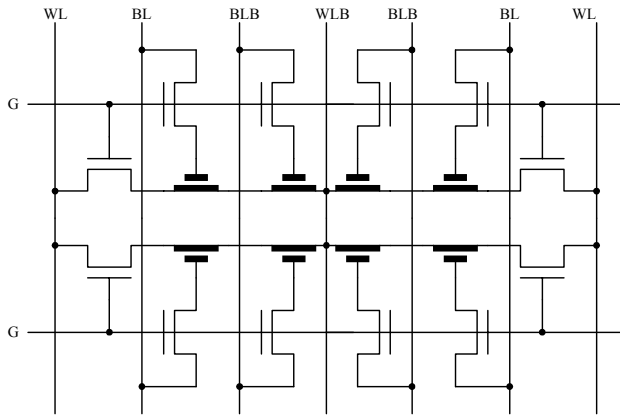


Figure 9. Schematic of a 4-cell cluster of differential SSDT cells. This cluster of mirrored cells optimizes the cell layout, yielding a more efficient use of die area.

5. CONCLUSIONS

This paper has described a new MRAM design that uses a sandwich-tunneling bit. The unique write properties of this bit eliminate the high power and uniformity problems that have plagued previous MRAM designs. Design and layout of a 256k MRAM, using the SSDT bit, have been completed. This MRAM design is based on an SRAM design, and retains the die size and pin-out of the SRAM device.

The write process of the SSDT bit, using a scissoring current that passes through the bit and produces closed flux switching in the antiferromagnetically coupled sandwich, significantly lowers the write current requirement of the memory. Typical SDT designs use two write currents of about 4 mA each, while the SSDT design uses a single current of about 0.8 mA - an order of magnitude improvement. This lower current allows the memory to be smaller, because smaller transistors, metal lines, and contact arrays can be used to carry and switch the write current, and the overall chip to be lower power.

Coupled with the single write current design, the SSDT cell design includes a write current select transistor. This select transistor isolates the write current from all cells except the selected cell - there are not any half-select conditions during a write cycle. Because of this write current isolation, the cell's switching uniformity is nearly irrelevant to the yield of the memory. Cell uniformity has been the primary yield problem in the popular SDT memory designs - it won't be an issue for the SSDT

design, where a larger than required write current does not cause any problems for the write operation.

In the completed MRAM design, the SSDT cell layout matches the x and y pitch of the SRAM cell of the reference SRAM design. This allowed the MRAM to utilize overhead circuitry from the SRAM design, and to maintain the same die size and pad arrangement as the SRAM device. The resulting MRAM should provide a drop in, nonvolatile replacement for the SRAM device.

6. ACKNOWLEDGMENTS

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