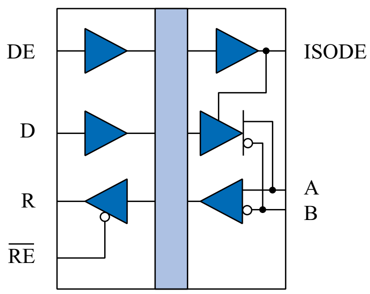
High-Speed Isolated 3.3 V Bus RS-485 Transceiver

Functional Diagram and Truth Table



IL3685P

V_{ID} (A-B)	DE	$\overline{RE}$	R	D	Mode	Notes
≥ 200 mV	L	L	H	X	Receive	
≤−200mV	L	L	L	X		
Open	L	L	H	X		A/B failsafe
≥ 1.5 V	H	L	H	H	Drive	R reads back D information
≤−1.5 V	H	L	L	L		
≥ 1.5 V	H	H	Z	H		R tri-state (no output)
≤−1.5 V	H	H	Z	L		
X	L	H	Z	X	Disabled	R tri-state; A/B failsafe

Features

- 3.3 V bus
- Up to 40 Mbps data rate
- 1/5 unit load (supports up to 160 nodes)
- Hot-plug capable
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- 44000 year barrier life
- 16.5 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- −40 °C to +85 °C temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- 600 V_{RMS} working voltage
- 2500 V_{RMS} isolation voltage
- VDE 0884-17 certified and UL 1577 approved
- 0.3" True 8™ mm 16-pin SOIC package

Applications

- DC-DC convertor-powered busses
- Factory automation
- Industrial control networks
- Building environmental controls

Description

IL3685-Series galvanically isolated, high-speed differential bus transceivers are designed for bidirectional data communication on balanced transmission lines. The devices use NVE's patented* spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The IL3685P delivers at least 1.5 V into a 54 Ω load for excellent data integrity over long cable lengths. The device is compatible with 3.3 V RS-485 busses and 3.3 V or 5 V controller interfaces.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

IsoLoop® is a registered trademark of NVE Corporation.
*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. F

Absolute Maximum Ratings[7]

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Voltage Range at A or B Bus Pins		–7		12	V	
Supply Voltage[1]	V_{DD1}, V_{DD2}	–0.5		7	V	
Digital Input Voltage		–0.5		V_{DD} + 0.5	V	
Digital Output Voltage		–0.5		V_{DD} + 1	V	
ESD (bus nodes)		16.5			kV	Air gap Discharge per IEC61000-4-2

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltages	V_{DD1} V_{DD2}	3 3		5.5 3.6	V	
Ambient Operating Temperature	T_A	–40		85	°C	
Junction Temperature	T_J	–40		100	°C	
High-Level Digital Input Voltage	V_{IH}	2.4 3.0		V_{DD1}	V	V_{DD1} = 3.3 V V_{DD1} = 5.0 V
Low-Level Digital Input Voltage	V_{IL}	0		0.8	V	
Differential Input Voltage[2]	V_{ID}			+12 / –7	V	
High-Level Output Current (Driver)	I_{OH}			60	mA	
High-Level Digital Output Current (Receiver)	I_{OH}			8	mA	
Low-Level Output Current (Driver)	I_{OL}	–60			mA	
Low-Level Digital Output Current (Receiver)	I_{OL}	–8			mA	
Digital Input Signal Rise and Fall Times	t_{IR}, t_{IF}	DC Stable				

Insulation Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)		8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.013	0.016		mm	
Barrier Resistance	R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance	C_{IO}		7		pF	f = 1 MHz
Leakage Current			0.2		μA_{RMS}	240 V_{RMS}, 60 Hz
Comparative Tracking Index	CTI	≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) — AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) — DC	V_{IO}	1500			V_{DC}	At maximum operating temperature
Surge Immunity (“V” Version)	V_{IOSM}	12.8			kV_{PK}	Per IEC 61000-4-5
Barrier Life			44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	θ_{JA}		67		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	θ_{JC}		12		°C/W	Double-sided PCB in free air
Junction–Ambient Thermal Resistance	θ_{JA}		46		°C/W	2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	θ_{JC}		9		°C/W	2s2p PCB in free air per JESD51
Power Dissipation	P_D			1.5	W	

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10 (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.
- Working Voltage (V_{IORM}; pollution degree 2): 600 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180 °C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

- 2500 V rating.
- Each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second.
- Each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute.

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

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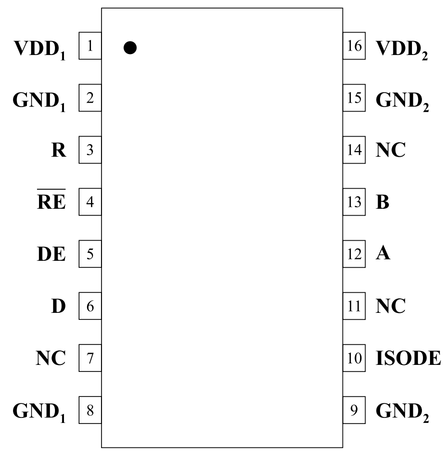
Pin Connections

1	V_{DD1}	Input power supply.
2	GND_1	Input power supply ground return (pin 2 is internally connected to pin 8).
3	R	Output data from bus.
4	$\overline{RE}$	Read data enable (if $\overline{RE}$ is high, R= high impedance).
5	DE	Drive enable.
6	D	Data input to bus.
7	NC	No internal connection.
8	GND_1	Input power supply ground return (pin 8 is internally connected to pin 2).
9	GND_2	Output power supply ground return (pin 9 is internally connected to pin 15).
10	ISODE	Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored.
11	NC	No internal connection.
12	A	Non-inverting bus line.
13	B	Inverting bus line.
14	NC	No internal connection.
15	GND_2	Output power supply ground return (pin 15 is internally connected to pin 9).
16	V_{DD2}	Output power supply.



Driver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD} = 3 V to 3.6 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Output voltage	V_O			V_{DD}	V	$I_O = 0$
Differential Output Voltage(2)	$\lvert V_{OD1}\rvert$			V_{DD}	V	$I_O = 0$
Differential Output Voltage(2)	$\lvert V_{OD2}\rvert$	1.5	2.1	3.5	V	R_L = 54 Ω
Differential Output Voltage(2)	V_{OD3}	1.5	2.1	3.5	V	R_L = 60 Ω; −7 V < V_{CM} < 12 V
Change in Magnitude of Differential Output Voltage(4)	$\Delta\lvert V_{OD}\rvert$			±0.2	V	R_L = 54 Ω or 100 Ω
Common Mode Output Voltage	V_{OC}			3	V	R_L = 54 Ω or 100 Ω
Change in Magnitude of Common Mode Output Voltage(4)	$\Delta\lvert V_{OC}\rvert$			±0.2	V	R_L = 54 Ω or 100 Ω
High Level Input Current	I_{IH}			10	μA	V_I = 3.5 V
Low Level Input Current	I_{IL}			−10	μA	V_I = 0.4 V
Absolute |Short-circuit Output Current|	I_{OS}			250	mA	−7 V < V_O < 12 V

Receiver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD2} = 3.0 V to 3.6 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Positive-going Input Threshold Voltage	V_{IT+}			0.2	V	−7 V < V_{CM} < 12 V
Negative-going Input Threshold Voltage	V_{IT-}	−0.2			V	−7 V < V_{CM} < 12 V
Hysteresis Voltage ($V_{IT+} - V_{IT-}$)	V_{HYS}		28		mV	V_{CM} = 0 V, T = 25°C
Differential Bus Input Capacitance	C_D		9	12	pF	
High Level Digital Output Voltage	V_{OH}	V_{DD} – 0.2	V_{DD}		V	V_{ID} = 200 mV I_{OH} = −20 μA
Low Level Digital Output Voltage	V_{OL}			0.2	V	V_{ID} = −200 mV I_{OH} = 20 μA
High-impedance-state output current	I_{OZ}			±1	μA	V_O = 0.4 to (V_{DD2}–0.5) V
Line Input Current	I_I			220	μA	V_I = 12 V
				−160	μA	V_I = −7 V
Input Resistance	R_I	60			kΩ	

Switching Characteristics

V_{DD1} = 5 V, V_{DD2} = 3.3 V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		40			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay(5)	t_{PD}		20	30	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew(6)	$t_{SK}(P)$		1	5	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Skew Limit(3)	$t_{SK}(LIM)$		2	10	ns	R_L = 54 Ω, C_L = 50 pF
Output Enable Time To High Level	t_{PZH}		15	30	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		15	30	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		15	30	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		15	30	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/μs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
V_{DD1} = 3.3 V, V_{DD2} = 3.3 V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		40			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay(5)	t_{PD}		25	35	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew(6)	$t_{SK}(P)$		2	5	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Skew Limit(3)	$t_{SK}(LIM)$		4	10	ns	R_L = 54 Ω, C_L = 50 pF
Output Enable Time To High Level	t_{PZH}		17	30	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		17	30	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		17	30	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		17	30	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/μs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns

Power Consumption

T_{min} to T_{max} and V_{DD2} = 3.0 V to 3.45 V unless otherwise stated						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Controller-Side Quiescent Supply Current V_{DD1} = 3.3 V V_{DD1} = 5 V	I_{DD1}		1 2	2 6	mA	f_{IN} = 0 Hz
Bus-Side Quiescent Supply Current	I_{DD2}		4	6	mA	R_T = ∞; Outputs Enabled; f_{IN} = 0 Hz
Controller-Side Dynamic Supply Current	I_{DD1}		0.18		mA/Mbps	V_{DD1} = 3.3 V
Bus-Side Dynamic Supply Current	$\Delta I_{DD2}/\Delta f_{IN}$		0.75		mA/Mbps	R_T = ∞
			0.55			R_T = 60 Ω
Transceiver Power Dissipation	I_{DD1} x V_{DD1} + I_{DD2} x V_{DD2}		17		mW	R_T = ∞; f_{IN} = 0 Hz
			150			R_T=60 Ω; f_{IN}=40 Mbps; excludes R_T power dissipation

Magnetic Field Immunity(8)

V_{DD1} = 5 V, V_{DD2} = 5 V						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50 Hz / 60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			
V_{DD1} = 3.3 V, V_{DD2} = 5 V						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50 Hz/ 60 Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Notes:

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
5. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
6. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
7. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 8.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 8).

GMR Isolator Operation

An equivalent circuit for each of the Giant Magnetoresistor (GMR) isolator channels is shown in Figure 2:

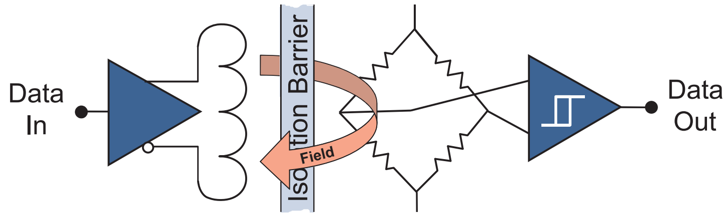


Figure 1. Isolator model signal path.

Isolator Signal Path
The GMR isolator signal path starts with a buffered input signal that is driven through an ultraminiature coil. This generates a small magnetic field that changes the electron spin polarization of GMR resistors, which are configured as a Wheatstone bridge. The change in spin polarization of the resistors creates a bridge voltage which drives an output comparator to construct an isolated version of the input signal.

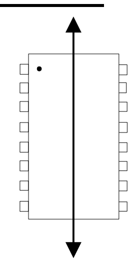
Small Size, High Speed, and Low EMI
The coil, GMR, and circuitry are integrated to allow small packages. GMR is inherently high speed and low distortion, and unlike transformers, does not rely on energy transfer, so power is low and EMI emissions are minimal.

High Magnetic Immunity
GMR provides large signals which improve magnetic immunity, and the Wheatstone bridge configuration cancels ambient common-mode magnetic fields, further enhancing immunity to external magnetic fields.

Electromagnetic Compatibility

IL3685-Series Transceivers are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is “end-to-end” (rather than to “pin-to-pin”) as shown in the diagram at right:



Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Power Supply Decoupling

V_{DD1} and V_{DD2} should be bypassed with 100 nF ceramic capacitors as close as possible to V_{DD} pins.

DC Correctness

The IL3685 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on Page 1. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

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Typical Performance Graphs

The following graphs show typical performance (25 °C; $V_{DD1} = V_{DD2} = 3.3$ V unless otherwise stated):

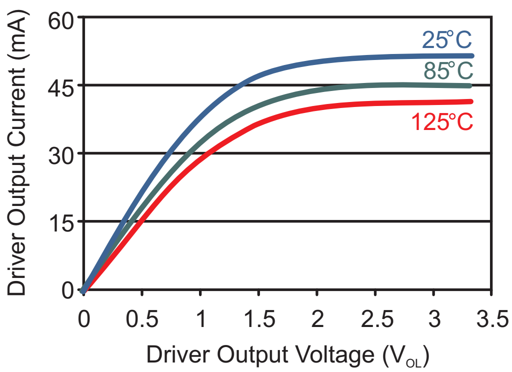

Figure 3. Typ. driver output current vs. driver output voltage (V_{OL}).

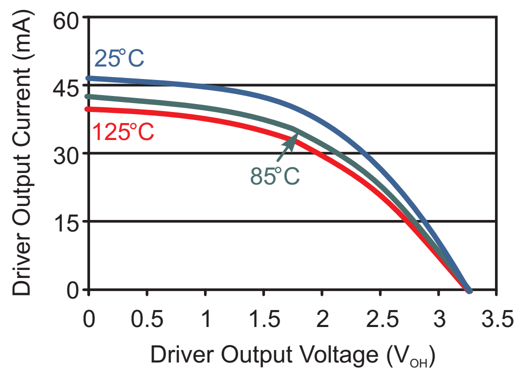

Figure 4. Typ. driver output current vs. driver output voltage (V_{OH}).

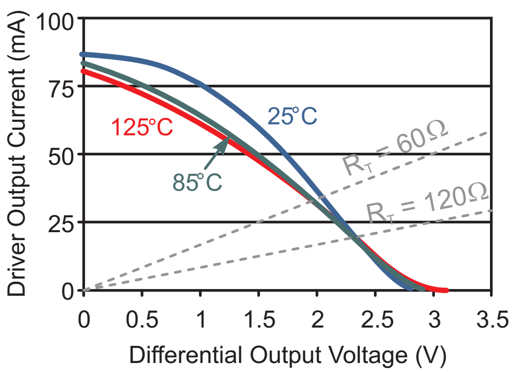

Figure 5. Driver output current versus differential output voltage

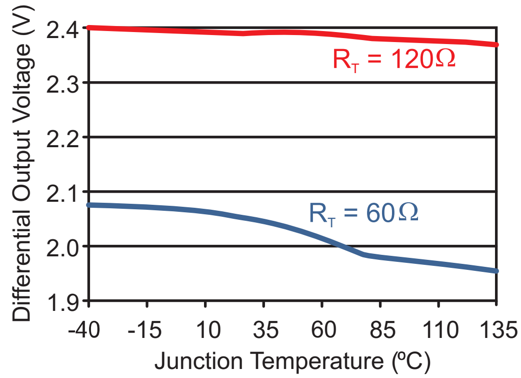

Figure 6. Driver differential output voltage versus junction temperature.

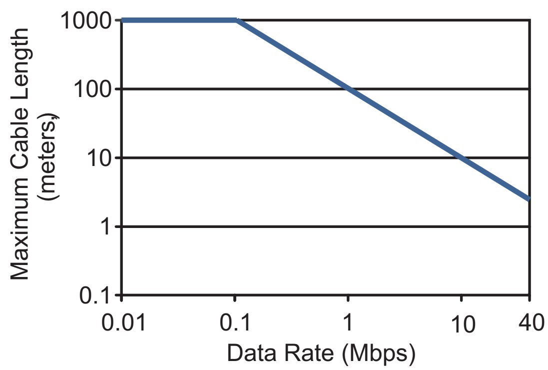

Figure 7. Maximum cable length versus data rate.

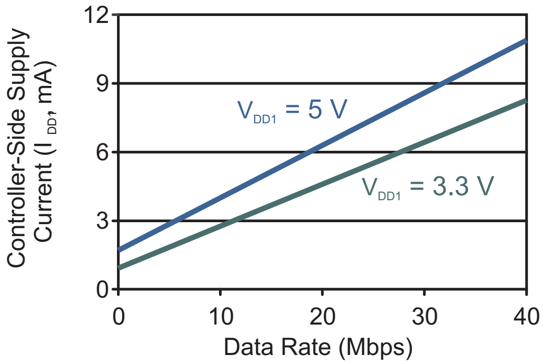

Figure 8. Typical controller-side supply current (I_{DD2}) versus data rate.

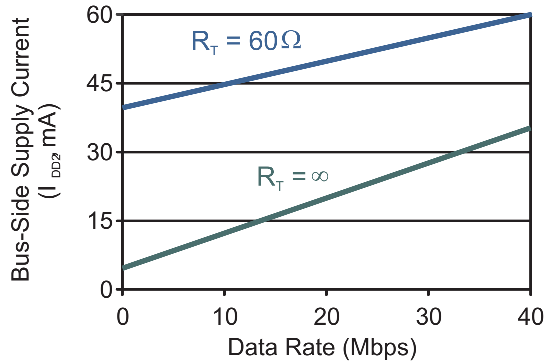

Figure 9. Typical bus-side supply current (I_{DD2}) versus data rate.

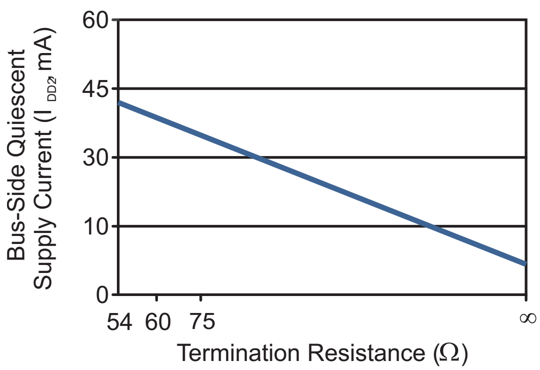

Figure 10. Typical bus-side supply current (I_{DD2}) versus aggregate termination resistance.

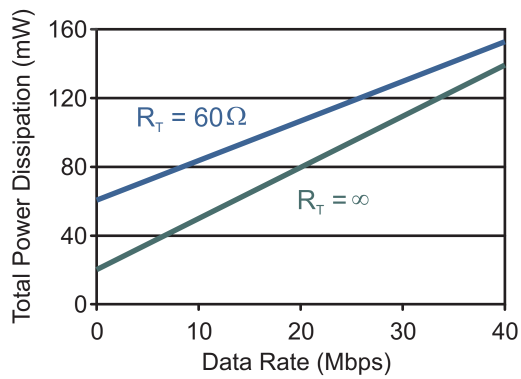

Figure 11. Typical transceiver power dissipation versus data rate (excludes R_T power dissipation).

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Application Information

The transceiver block diagram is shown below:

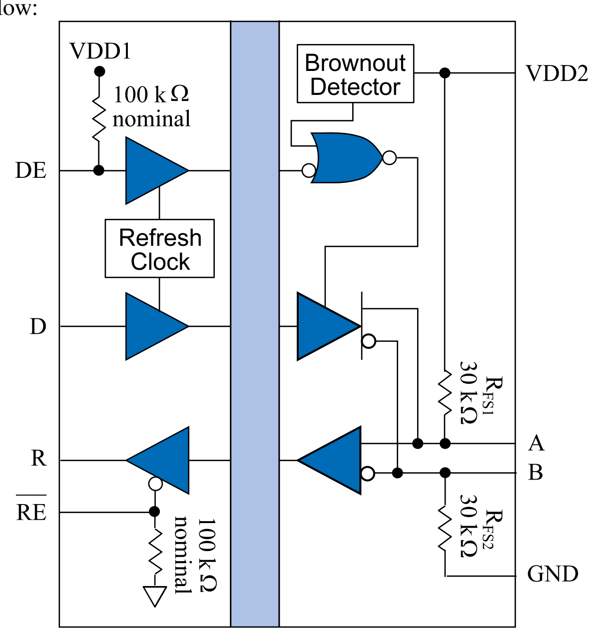


Figure 12. Detailed transceiver block diagram.

Receiver Features

The receiver output "R" has tri-state capability via the active low $\overline{\text{RE}}$ input.

Driver Features

The driver features low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

True 3.3-volt Bus Operation

IL3685P transceivers are guaranteed to provide the minimum differential voltages with a 3.0-volt bus supply, providing true 3.3-volt bus operation with ample design margins.

Deterministic Power Up and Brownout Detection

The parts have circuitry to disable the bus driver until the driver-side voltage (VDD2) reaches approximately 2.5 volts on power-up. The transceiver is disabled when the voltage drops below approximately 2.3 volts on power-down. This brownout circuitry ensures the transceiver does not "crash" the bus on power up, power down, or brownout, and eliminates the need for external power supply monitors. In addition, a patented refresh circuit maintains the correct transceiver output state with respect to data input (DC correctness). The refresh circuit ensures the bus outputs will follow the Function Table shown on Page 1 after power up.

Hot Plug Operation

Deterministic power-up allows IL3685P nodes to "hot plug" into the bus, since the bus driver will be in a high-impedance state until the bus supply is enough for the bus driver to operate.

Unpowered Nodes

Unpowered nodes (i.e., no VDD2 power) revert to high impedance on the "A" and "B" bus lines and will not disturb bus operation.

Internal Fail-Safe Biasing Resistors

Internal "fail-safe biasing" forces a logic high state on "R" with an open-circuit between the bus "A" and "B" lines, or when no drivers are active on the bus.

Receiver Data Rate, Cables and Terminations

Shielded twisted pair bus cable is recommended for high transmission speeds (more than 500 Kbps). IL3685-Series transceivers are intended for networks up to 1,000 meters shielded twisted pair proper termination. The maximum data rate decreases as cable length increases. Unshielded or untwisted can be at used at low baud rates and short distances.

Typical Application

The following schematic shows a typical isolated RS-485 bus power supply and node:

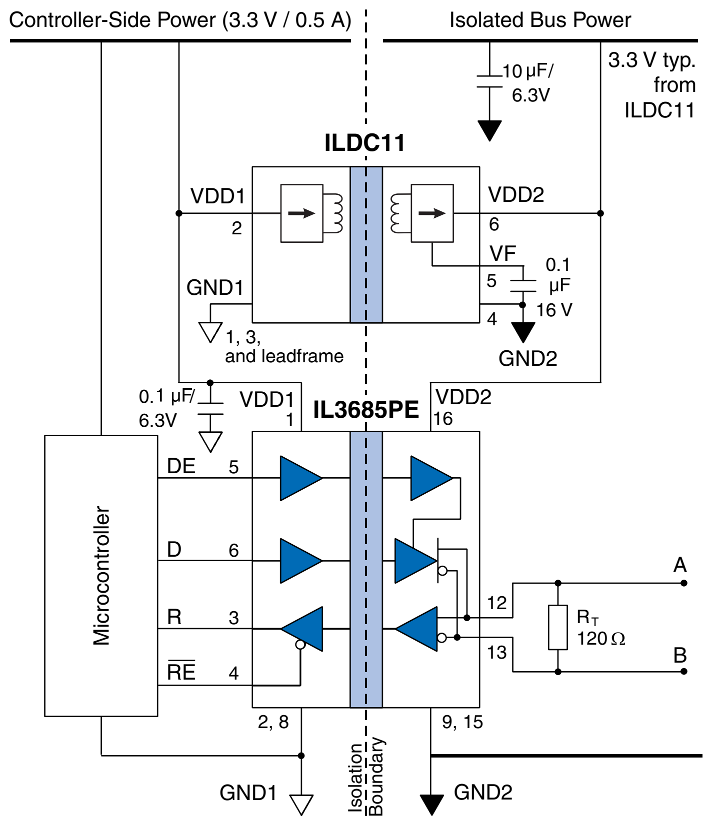
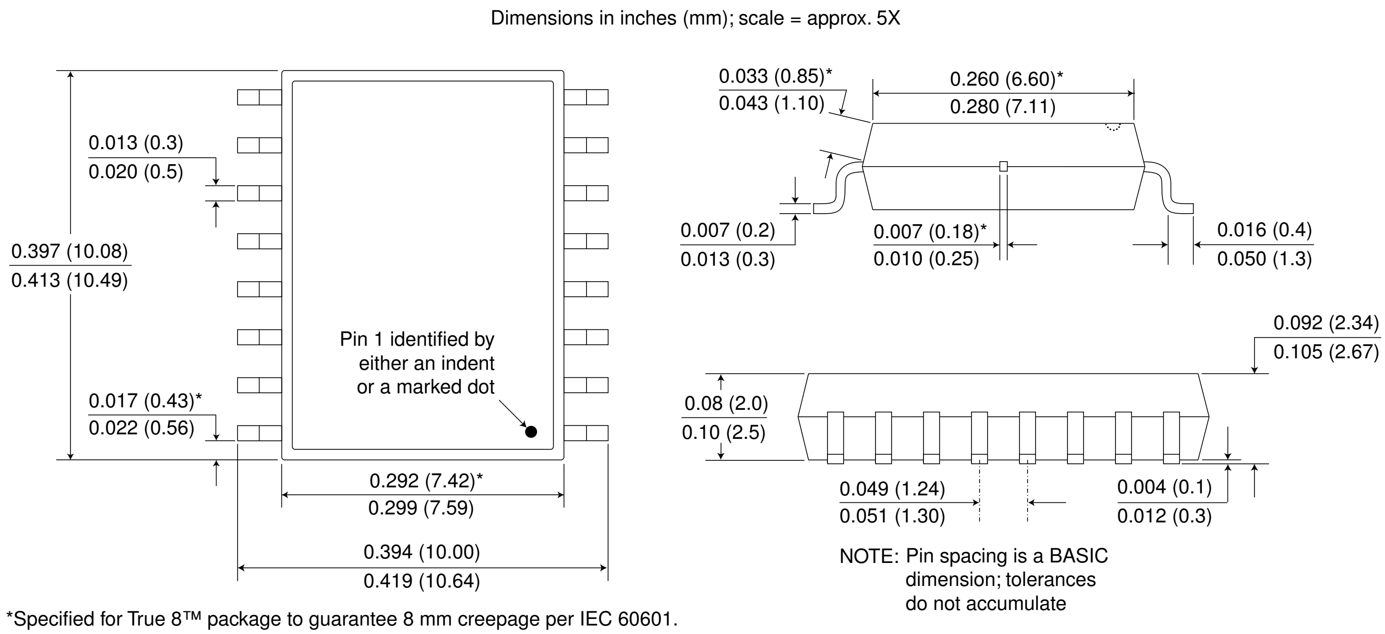
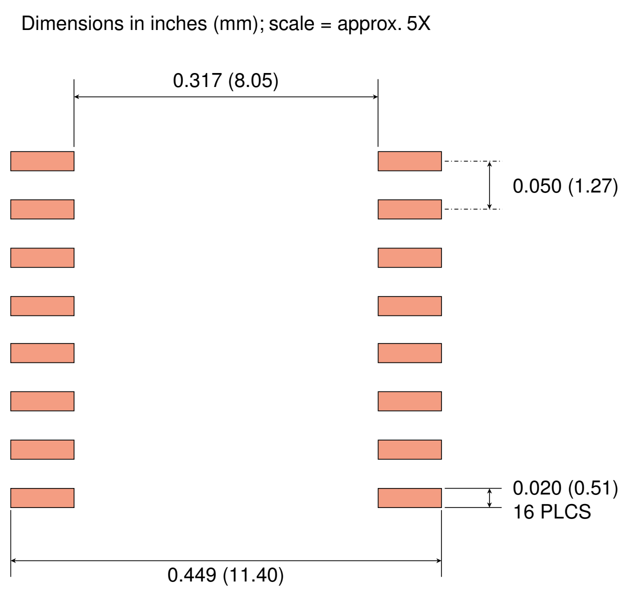


Figure 13. Typical circuit for isolated RS-485 bus supply and node.

Package Drawing



Recommended Pad Layout



Ordering Information and Valid Part Numbers

IL 36 85 P E TR13

Bulk Packaging
Blank = Tube
TR13 = 13" Tape and Reel

Package
E = RoHS Compliant 0.3" SOIC

Variant Designator
P = 3.3V Bus Version

Channel Configuration
85 = RS-485

Base Part Number
36 = High-Speed Transceiver

Product Family
IL = Isolators

Valid Part Numbers
IL3685PE
IL3685PE TR13

RoHS COMPLIANT

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Revision History

ISB-DS-001-IL3685P-F
October 2022

Changes

- Clarified truth table (p. 1).
- Upgraded to IEC 60747-17 (VDE 0884-17):2021-10 (p. 3).
- GMR operation overview (p. 8).
- Additional performance graphs (p. 9).

ISB-DS-001-IL3685P-E
May 2020

Change

- More details on power up, hot plug, and brownout detection.

ISB-DS-001-IL3685P-D
March 2020

Changes

- Updated VDE certification to VDE V 0884-11.
- Deleted PROFIBUS logo since the IL3685P is typically PROFIBUS compliant but not guaranteed.
- Updated EMC specifications (p. 8).
- Added maximum cable length versus data rate Typical Performance Graph (p. 9).
- Added DC-DC convertor reference design (p. 11).
- Misc. minor changes.

ISB-DS-001-IL3685P-C
December 2019

Changes

- Broke out power consumption specifications in separate table; tightened specs (p. 7).
- Added typical performance charts for power vs. speed (p. 8).

ISB-DS-001-IL3685P-B
November 2019

Changes

- Corrected Recommended Operating Conditions—Supply Voltage—V_{DD2} (p. 2).
- Updated Thermal Characteristics (p. 2).
- Cosmetic changes and rewrites (p. 7).

ISB-DS-001-IL3685P-A
December 2017

Changes

- Revised thermal specifications.
- Initial release.

ISB-DS-001-IL3685P-PRELIM
May 2017

Change

- Preliminary release.

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ISB-DS-001-IL3685P-F

October 2022