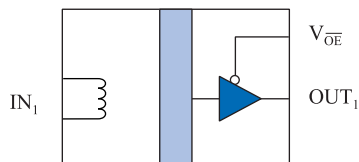
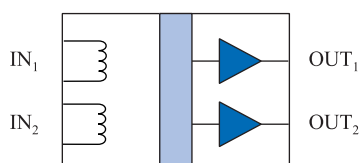


Ultrahigh CMTI Isolated MOSFET Drivers

Functional Diagrams



IL610CMTI



IL611CMTI

Features

- 200 kV/ μ s guaranteed CMTI; 300 kV/ μ s with deglitch
- Extended 3 V to 6.6 V power supply range
- Switching frequencies up to 50 Mhz
- Flexible inputs with wide input voltage range
- Input current as low as 5 mA
- No input-side power supply needed
- No reverse input protection needed
- Failsafe output (high output for zero coil current)
- No carrier or clock for low EMI emissions and susceptibility
- Extremely high EMI and magnetic immunity
- 2.5 kV isolation; up to 800 V_{RMS} Working Voltage
- IEC 60747-17 (VDE 0884-17):2021-10; UL 1577
- 44000 year barrier life
- Single and dual-channel configurations
- 8-pin MSOP and SOIC packages

Applications

- H-bridges
- Floating supply applications
- Noisy environments

Description

The IL600-Series isolators are passive input digital signal isolators with CMOS outputs. The IL6xxCMTI version is optimized for driving MOSFETs either directly or with an external gate driver.

Resistors set the input current, and five milliamps guarantees switching. The inputs can be configured as non-inverting or inverting.

CMTI-grade isolators are 100% tested to ensure each part has at least 200 kV/ μ s minimum Common-Mode Transient Immunity. Simple external deglitch circuitry can extend the CMTI to an extraordinary 350 kV/ μ s typical.

The parts also have an extended supply range of up to 6.6 volts for compatibility to directly drive a range of power MOSFETs or gate driver ICs.

The devices are manufactured with NVE's patented* IsoLoop[®] spintronic Giant Magnetoresistive (GMR) technology for small size, high speed, and low power.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Absolute Maximum Ratings⁽¹⁾

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---------------------------------------|-----------------|--------------------|------|----------------------|-------|-----------------|
| Storage Temperature | T _S | -55 ⁽²⁾ | | 150 | °C | |
| Ambient Operating Temperature | T _A | -40 ⁽³⁾ | | 85 | °C | |
| Supply Voltage | V _{DD} | -0.5 | | 7 | V | |
| DC Input Current | I _{IN} | -25 | | 25 | mA | |
| AC Input Current (Single-Ended Input) | I _{IN} | -35 | | 35 | mA | |
| AC Input Current (Differential Input) | I _{IN} | -75 | | 75 | mA | |
| Output Voltage | V _O | -0.5 | | V _{DD} +1.5 | V | |
| Maximum Output Current | I _O | -10 | | 10 | mA | |
| ESD | | | 2 | | kV | HBM |

Note 1: Operating at absolute maximum ratings will not damage the device. Parametric performance is not guaranteed at absolute maximum ratings.

Recommended Operating Conditions

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|--|-----------------------------------|--------------------|------|------------------|------------------|-----------------|
| Ambient Operating Temperature | T _A | -40 ⁽³⁾ | | 85 | °C | |
| Supply Voltage | V _{DD} | 3 | | 6 | V | |
| Input Signal Rise and Fall Times | t _{IR} , t _{IF} | | | 1 | μs | |
| V _{OE} Logic High Input Voltage | V _{IH} | 2.4 | | V _{DD1} | V | |
| V _{OE} Logic Low Input Voltage | V _{IL} | 0 | | 0.8 | V | |
| Common Mode Input Voltage | V _{CM} | | | 1000 | V _{RMS} | |

Insulation Specifications

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|--|-----------------------------|--------------|-------------------|------|-------------------------------------|---|
| Creepage Distance (external) | | | | | | |
| MSOP8 | | 3.01 | | | mm | |
| SOIC8 | | 4.03 | | | mm | |
| Total Barrier Thickness (internal) | | 0.012 | 0.013 | | mm | |
| Leakage Current | | | 0.2 | | μA | 240 V _{RMS} , 60 Hz |
| Barrier Resistance | R _{IO} | | >10 ¹⁴ | | | 500 V |
| Barrier Capacitance | C _{IO} | | 7 | | Ω pF | f = 1 MHz |
| Comparative Tracking Index | CTI | ≥175 | | | V | Per IEC 60112 |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | AC DC V _{IO} | 1000 1500 | | | V _{RMS} V _{DC} | At maximum operating temperature |
| Barrier Life | | | 44000 | | Years | 100°C, 1000 V _{RMS} , 60% CL activation energy |

Thermal Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|--|-----------------|------|------------|------------|-------|--|
| Junction–Ambient Thermal Resistance | θ _{JA} | | 184 134 | | °C/W | Soldered to double-sided board; free air |
| Junction–Case (Top) Thermal Resistance | θ _{JT} | | 15 10 | | °C/W | |
| Power Dissipation | P _D | | | 500 675 | mW | |

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10 (Basic Isolation; VDE File Number 5016933-4880-0001):

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit
- Working Voltage (V_{IORM} ; pollution degree 2):

| Package | Part No. Suffix | Working Voltage |
|---------|-----------------|-----------------|
| MSOP8 | -1 | 800 V_{RMS} |
| SOIC8 | -3 | 700 V_{RMS} |

| Safety-Limiting Values | Symbol | Value | Units |
|--|--------|-------|-------------|
| Safety rating ambient temperature | T_S | 180 | $^{\circ}C$ |
| Safety rating power (180 $^{\circ}C$) | P_S | 270 | mW |
| Supply current safety rating (total of supplies) | I_S | 54 | mA |

UL 1577 (Component Recognition Program File Number E207481)

- 2500 V rating.
- Each part tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute.

Soldering Profile

Per JEDEC J-STD-020C; MSL 1

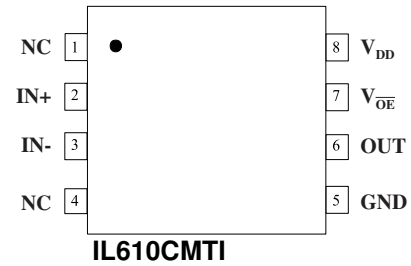
Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Pin Connections

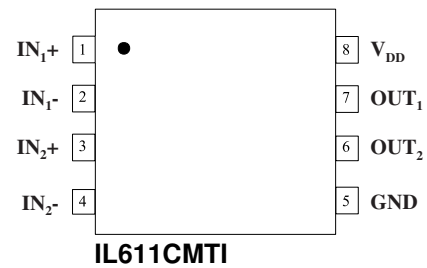
IL610CMTI

| | | |
|---|-----------------|---|
| 1 | NC | No internal connection |
| 2 | IN+ | Coil connection |
| 3 | IN- | Coil connection |
| 4 | NC | No internal connection |
| 5 | GND | Ground return for V _{DD} |
| 6 | OUT | Data out |
| 7 | V _{OE} | Output enable. Internally held low with 100 kΩ |
| 8 | V _{DD} | Supply Voltage |



IL611CMTI

| | | |
|---|------------------|-----------------------------------|
| 1 | IN ₁₊ | Channel 1 coil connection |
| 2 | IN ₁₋ | Channel 1 coil connection |
| 3 | IN ₂₊ | Channel 2 coil connection |
| 4 | IN ₂₋ | Channel 2 coil connection |
| 5 | GND | Ground return for V _{DD} |
| 6 | OUT ₂ | Data out, channel 2 |
| 7 | OUT ₁ | Data out, channel 1 |
| 8 | V _{DD} | Supply Voltage |



Operating Specifications

| Coil Specifications ($V_{DD} = 3\text{ V} - 6.6\text{ V}$; $T = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ unless otherwise stated) | | | | | | |
|--|---------------|------|------|------|---------------------------|--|
| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Coil Input Resistance | R_{COIL} | 47 | 85 | 112 | Ω | $T = 25^{\circ}\text{C}$ |
| | | 31 | 85 | 128 | Ω | $T = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ |
| Coil Resistance Temperature Coefficient | $TC R_{COIL}$ | | 0.2 | 0.25 | $\Omega/^{\circ}\text{C}$ | |
| Coil Inductance | L_{COIL} | | 9 | | nH | |

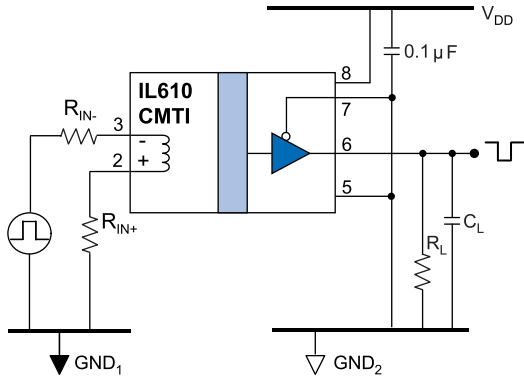


Figure 1. Test circuit.

5 V Specifications

| 5 V Electrical Specifications ($V_{DD} = 4.5\text{ V} - 6.6\text{ V}$; $T = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ unless otherwise stated) | | | | | | |
|--|-------------------------------------|------|--------|------|----------|--|
| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Quiescent Supply Current | | | | | | |
| IL610CMTI | I _{DD} | | 2 | 3 | mA | $V_{DD} = 5\text{ V}$, $I_{IN} = 0$ |
| IL611CMTI | | | 4 | 6 | | |
| Input Threshold | I _{INH-DC} | 0.5 | 3 | | mA | |
| Input Threshold Hysteresis | I _{INH} - I _{INL} | 0.25 | 1 | | mA | $V_{DD} = 5\text{ V}$ |
| | | 0.25 | 0.5 | | | $V_{DD} = 6\text{ V}$ |
| Failsafe Input Current ⁽¹⁾ | I _{FS-HIGH} | -25 | | 0.5 | mA | |
| | I _{FS-LOW} | 5 | | 25 | mA | |
| High Output Voltage | V _{OH} | 4.9 | 4.999 | | V | $V_{DD} = 5\text{ V}$, $I_O = 20\ \mu\text{A}$ |
| | | 4.0 | 4.8 | | V | $V_{DD} = 5\text{ V}$, $I_O = 4\text{ mA}$ |
| Low Output Voltage | V _{OL} | | 0.0007 | 0.1 | V | $V_{DD} = 5\text{ V}$, $I_O = -20\ \mu\text{A}$ |
| | | | 0.12 | 0.8 | V | $V_{DD} = 5\text{ V}$, $I_O = -4\text{ mA}$ |
| Output Stage High-Side Drain-to-Source Resistance | R _{DS-P} | | 40 | | Ω | $V_{DD} = 5\text{ V}$ |
| | | | 38 | | | $V_{DD} = 6\text{ V}$ |
| Output Stage Low-Side Drain-to-Source Resistance | R _{DS-N} | | 30 | | Ω | $V_{DD} = 5\text{ V}$ |
| | | | 28 | | | $V_{DD} = 6\text{ V}$ |
| Output Short-Circuit Current | I _{scI} | 40 | 55 | 70 | mA | $V_{DD} = 5\text{ V}$ |
| | | 45 | 65 | 80 | | $V_{DD} = 6\text{ V}$ |

| 5 V Switching Specifications ($V_{DD} = 4.5\text{ V} - 6.6\text{ V}$; $T = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ unless otherwise stated) | | | | | | |
|---|------------------|------|------|------|------------------------|--|
| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Minimum Pulse Width ⁽¹⁾ | PW | 10 | | | ns | Digital Drive: R _L = 1 K Ω ; C _L = 15 pF; t _{IR} = t _{IF} = 3 ns |
| Propagation Delay Input to Output (High-to-Low) | t _{PHL} | | 8 | 15 | ns | |
| Propagation Delay Input to Output (Low to High) | t _{PLH} | | 8 | 15 | ns | |
| Average Propagation Delay Drift | t _{PLH} | | 10 | | ps/ $^{\circ}\text{C}$ | |
| Pulse Width Distortion t _{PHL} - t _{PLH} ⁽²⁾ | PWD | | 3 | 5 | ns | |
| Pulse Jitter | t _J | | | 100 | ps | |
| Propagation Delay Skew ⁽³⁾ | t _{PSK} | -2 | | 2 | ns | |
| Output Rise Time (10-90%) | t _R | | 2 | 4 | ns | |
| Output Fall Time (10-90%) | t _F | | 2 | 4 | ns | |
| Minimum Pulse Width ⁽¹⁾ | PW | 75 | | | ns | |
| Propagation Delay Input to Output (High-to-Low) | t _{PHL} | | 50 | 70 | ns | Driving high-power MOSFET; R _L = 1 M Ω ; C _L = 1000 pF; t _{IR} = t _{IF} = 3 ns |
| | | | 60 | 90 | | |
| Propagation Delay Input to Output (Low to High) | t _{PLH} | | 60 | 90 | | |
| Pulse Width Distortion t _{PHL} - t _{PLH} ⁽²⁾ | PWD | | 30 | 50 | | |
| Output Rise Time (10-90%) | t _R | | 130 | 160 | | |
| Output Fall Time (10-90%) | t _F | | 110 | 140 | | |

| 5 V Common Mode Transient Immunity Specifications ($V_{DD} = 4.5\text{ V} - 6.6\text{ V}$; $T = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ unless otherwise stated) | | | | | | |
|--|--------------------------------------|--------------------|-----|--|-------------------|-------------------------------|
| IL610CMTI (single channel) | | | | | | |
| 5 mA drive | I _{CMH} , I _{CM L} | | 165 | | kV/ μs | I _{COIL} = 0/ +5 mA |
| 10 mA drive ⁽²⁾ | | 200 ⁽²⁾ | 240 | | | I _{COIL} = 0/ +10 mA |
| With external deglitching | | 300 | 350 | | | 10 ns output deglitch |

| | | | | | | |
|--------------------------------|--------------------------------------|--------------------|-----|--|-------------------|-------------------------------|
| IL611CMTI (two channel) | | | | | | |
| 5 mA drive | I _{CMH} , I _{CM L} | | 145 | | kV/ μs | I _{COIL} = 0/ +5 mA |
| 10 mA drive ⁽²⁾ | | 200 ⁽²⁾ | 210 | | | I _{COIL} = 0/ +10 mA |
| With external deglitching | | 300 | 350 | | | 10 ns output deglitch |

3.3 V Specifications

| 3.3 V Electrical Specifications (V _{DD} = 3 V – 3.6 V; T = –40°C – 85°C unless otherwise stated) | | | | | | |
|---|-------------------------------------|------|--------|--------|-------|--|
| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Quiescent Supply Current | | | | | | |
| IL610 | I _{DD} | | 1.3 | 2 | mA | V _{DD} = 3.3 V, I _{IN} = 0 |
| IL611 | I _{DD} | | 2.6 | 4 | | |
| Input Threshold | I _{INH-DC} | 0.3 | 1 | | mA | Single-ended Unipolar Bipolar Differential |
| | I _{INL-DC} | | 4 | 8 5 | | |
| Input Threshold Hysteresis | I _{INH} - I _{INL} | 0.25 | 3 | | mA | |
| Failsafe Input Current ⁽¹⁾ | I _{FS-HIGH} | -25 | | 0.3 | mA | |
| High Output Voltage | V _{OH} | 3.2 | 3.3 | | V | V _{DD} = 3.3 V, I _O = 20 μA |
| | | 3.0 | 3.28 | | V | V _{DD} = 3.3 V, I _O = 4 mA |
| Low Output Voltage | V _{OL} | | 0.0005 | 0.1 | V | V _{DD} = 3.3 V, I _O = -20 μA |
| | | | 0.15 | 0.8 | V | V _{DD} = 3.3 V, I _O = -4 mA |
| Output Stage High-Side Drain-to-Source Resistance | R _{DS-P} | | 55 | | Ω | |
| Output Stage Low-Side Drain-to-Source Resistance | R _{DS-N} | | 38 | | Ω | |
| Output Short-Circuit Current | I _{SC} | 15 | 25 | 40 | mA | |

| 3.3 V Switching Specifications (V _{DD} = 3 V – 3.6 V; T = –40°C – 85°C unless otherwise stated) | | | | | | |
|--|------------------|-----|-----|-----|-------|---|
| Minimum Pulse Width ⁽¹⁾ | PW | 10 | | | ns | Digital Drive: Test Circuit 2; R _L = 1 KΩ; C _L = 15 pF; t _{IR} = t _{IF} = 3 ns |
| Propagation Delay Input to Output (High to Low) | t _{PHL} | | 12 | 18 | ns | |
| Propagation Delay Input to Output (Low to High) | t _{PLH} | | 12 | 18 | ns | |
| Average Propagation Delay Drift | t _{PLH} | | 10 | | ps/°C | |
| Pulse Width Distortion t _{PHL} - t _{PLH} ⁽²⁾ | PWD | | 3 | 5 | ns | |
| Propagation Delay Skew ⁽³⁾ | t _{PSK} | -2 | | 2 | ns | |
| Output Rise Time (10–90%) | t _R | | 3 | 5 | ns | |
| Output Fall Time (10–90%) | t _F | | 3 | 5 | ns | |
| Minimum Pulse Width ⁽¹⁾ | PW | 100 | | | ns | MOSFET drive: Test Circuit 2; R _L = 1 MΩ; C _L = 1000 pF; t _{IR} = t _{IF} = 3 ns |
| Propagation Delay Input to Output (High-to-Low) | t _{PHL} | | 75 | 100 | ns | |
| Propagation Delay Input to Output (Low to High) | t _{PLH} | | 90 | 130 | | |
| Pulse Width Distortion t _{PHL} - t _{PLH} ⁽²⁾ | PWD | | 45 | 75 | | |
| Output Rise Time (10–90%) | t _R | | 200 | 240 | | |
| Output Fall Time (10–90%) | t _F | | 165 | 200 | | |

| 3.3 V Common Mode Transient Immunity Specifications (V _{DD} = 3 V – 3.6 V; T = –40°C – 85°C unless otherwise stated) | | | | | | |
|---|-------------------------------------|--|-----|--|-------|-------------------------------|
| IL610CMTI (single channel) | | | | | | |
| 5 mA drive | CM _H , CM _L | | 125 | | kV/μs | I _{COIL} = 0/ +5 mA |
| 10 mA drive | | | 175 | | | I _{COIL} = 0/ +10 mA |
| With external deglitching | | | 300 | | | 10 ns output deglitch |
| IL611CMTI (two channel) | | | | | | |
| 5 mA drive | CM _H , CM _L | | 110 | | kV/μs | I _{COIL} = 0/ +5 mA |
| 10 mA drive | | | 155 | | | I _{COIL} = 0/ +10 mA |
| With external deglitching | | | 300 | | | 10 ns output deglitch |

Notes:

- Failsafe Operation is defined as the guaranteed output state which will be achieved if the DC input current falls between the input levels specified. Note if Failsafe to Logic Low is required, the DC current supplied to the coil must be at least 8 mA using 3.3 V supplies versus 5 mA for 4.5 V or higher supplies.
- Minimum Pulse Width is the shortest pulse width at which the specified PWD is guaranteed.
- PWD is defined as |t_{PHL} - t_{PLH}|.
- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
- 100% tested.

Typical Performance Graphs

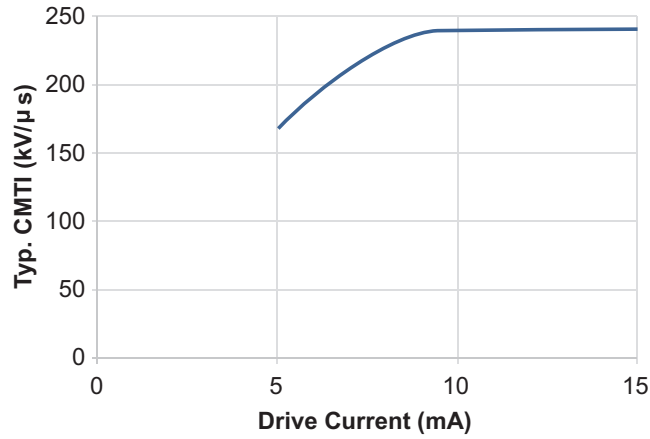


Figure 2. Typical CMTI vs. drive current ($V_{DD} = 5\text{ V}$).

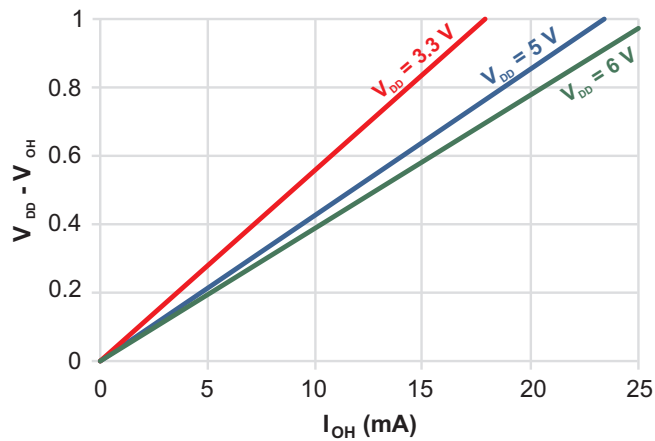


Figure 3. Typical high output voltage vs. load.

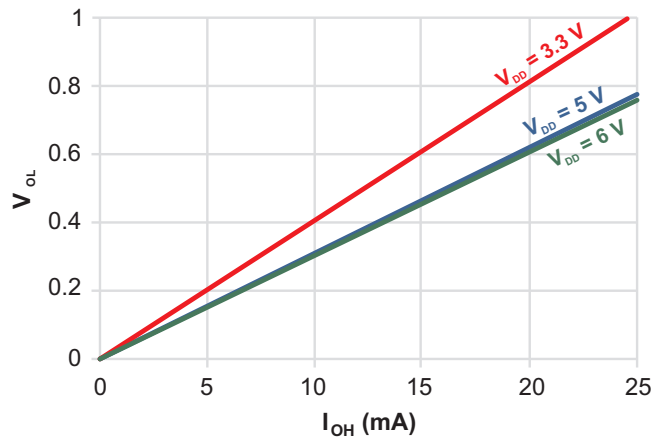


Figure 4. Typical low output voltage vs. load

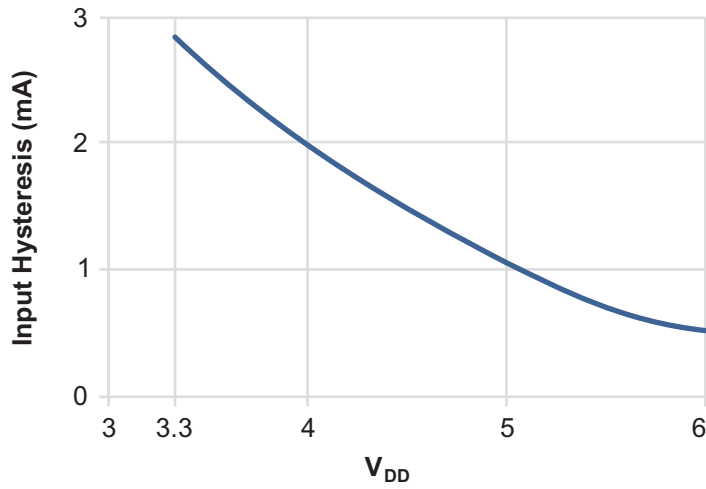


Figure 5. Typical input threshold current hysteresis.

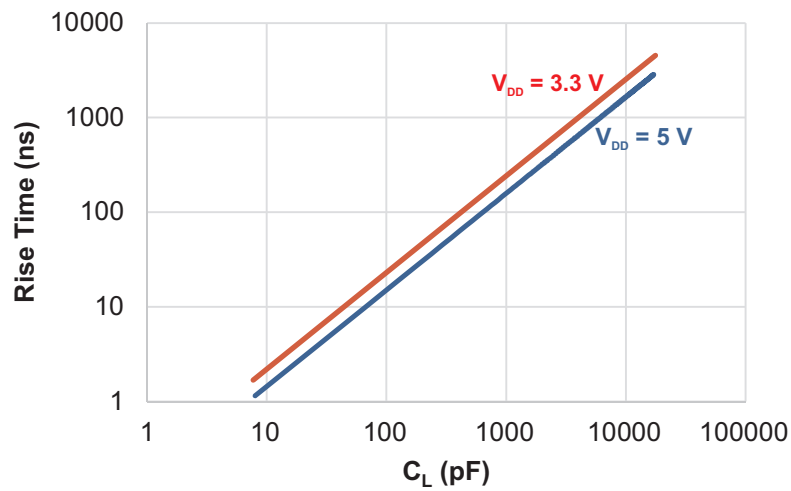


Figure 6. Typical output rise time vs. load capacitance

Applications Information

Overview

Figure 7 shows a block diagram of the IL61xCMTI. The coil, GMR, and support integrated circuitry are integrated on a single chip:

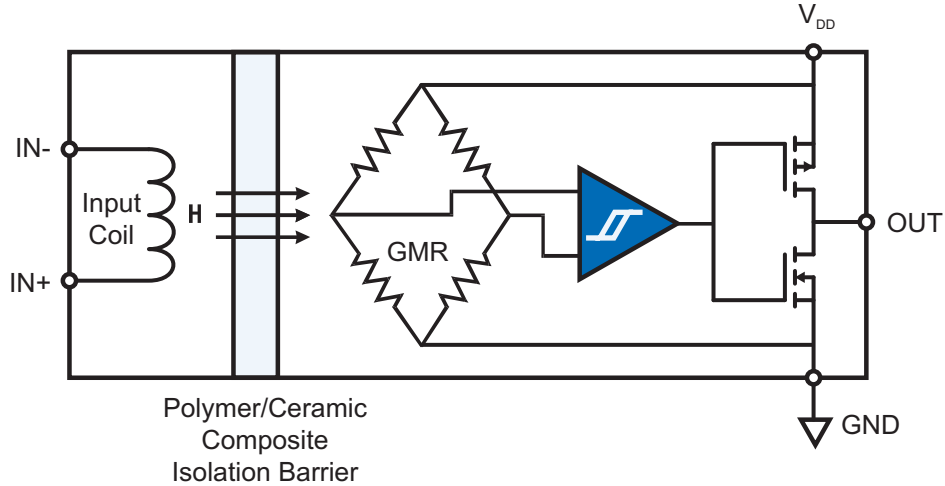


Figure 7. IL61xCMTI block diagram (each channel).

GMR Wheatstone Bridge

The heart of the Isolator is a Wheatstone bridge constructed of GMR resistor elements. The current in the coil driven from the input side of the isolator creates a magnetic field that switches the GMR in the bridge. Thus the signal is transmitted by magnetic field.

Schmitt Trigger and Output Stage

The change in the bridge is detected by a Schmitt trigger comparator. This drives a push-pull MOSFET output stage.

Input Coil

IL600-Series Isolators are current mode devices. Changes in current flow into the input coil result in logic state changes at the output. Input-stage hysteresis improves noise immunity. Output logic high is the zero input current state:

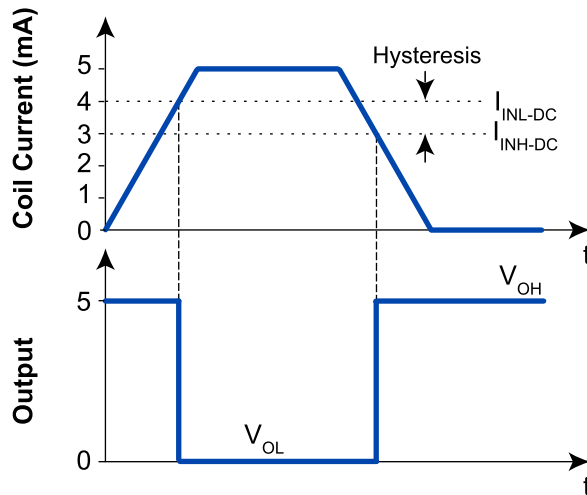


Figure 8. Typical IL600-Series transfer function.

Coil Polarity

The device switches to low if current flows from (In-) to (In+). *Note that the designations “In-“ and “In+” refer to logic levels, not current flow.* Positive values of current mean current flow into the In- input.

Input Resistor Selection

Resistors set the coil input current:

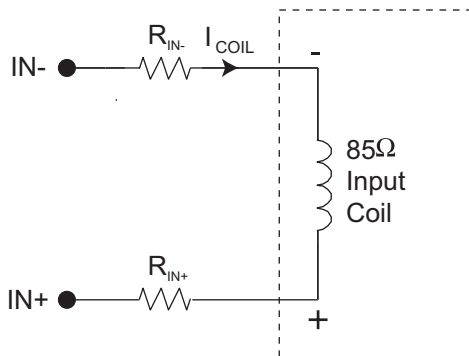


Figure 9. Input resistors.

There is no limit to input voltages because there are no semiconductor input structures.

The resistors can should be divided between the two inputs. The two resistors can be the same if necessary, although because of some inherent structural asymmetry, an R_{IN-} resistor approximately 50% larger than R_{IN+} is optimal for CMTI.

The worst-case drive current is calculated from the worst-case input voltage divided by the total series resistance plus the worst-case coil resistance. Note that coil resistance increases with temperature. Driver output impedance should also be considered if it is significant.

The following table summarizes typical input resistor values:

| V _{COIL} | 5 mA min. drive current | | 10 mA typical drive current | |
|-------------------|-------------------------|------------------|-----------------------------|------------------|
| | R _{IN-} | R _{IN+} | R _{IN-} | R _{IN+} |
| 3.3 V | 300 Ω | 200 Ω | 200 Ω | 140 Ω |
| 5 V | 500 Ω | 330 Ω | 250 Ω | 165 Ω |

Table 1. Typical input resistor values.

The values for 5 mA drive are designed to provide a minimum of 5 mA drive current so the isolator is guaranteed to switch. The values for 10 mA drive are designed to provide 10 mA typical drive current to maximize CMTI.

The worst-case logic low threshold current is 8 mA, which is for single-ended operation with a 3 V supply. With differential drive the logic low threshold current is 5 mA for the range of supplies.

Maximum Coil Current

Absolute Maximum unipolar coil current is 25 mA, while bipolar mode allows up to ±75 mA. The difference in specifications is due to the risk of electromigration of coil metals under constant current flow. Long-term unipolar DC current flow above 25 mA can cause erosion of the coil metal. In differential mode, erosion takes place in both directions as each current cycle reverses and has no net effect up to the absolute maximum current.

An advantage over optocouplers and other high-speed couplers in differential mode is that no reverse bias protection for the input structure is required for a differential signal.

Drive Configurations

IL600-Series Isolators can be configured in inverting (Figure 9) non-inverting (Figure 10) or bipolar (Figure 11) configurations.

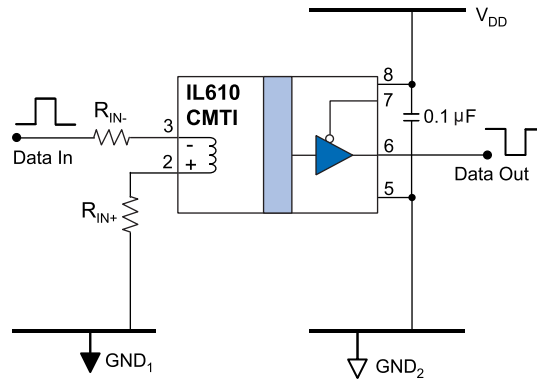


Figure 10. Inverting drive configuration.

This configuration is similar to standard logic. The output is high when the coil current is less than 0.5 mA, and low when the current is more than 5 mA.

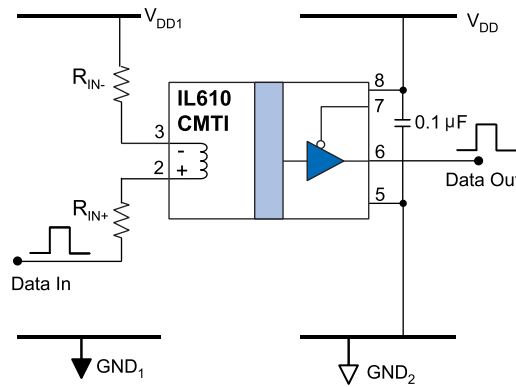


Figure 11. Non-inverting drive configuration.

When a logic high is applied to the input, the current through the coil is zero. When the input is a logic low (0 V), at least 5 mA flows through the coil from the In- side to the In+ side.

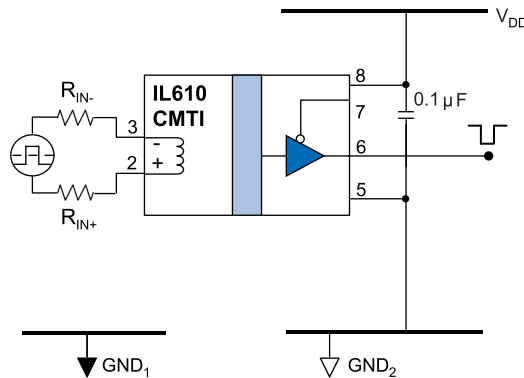


Figure 12. Bipolar drive configuration.

The differential coil current is negative for a high output and positive for a low output. Bipolar drive increases the absolute maximum coil current, minimizes the required input current with a 3.3-volt supply, and maximizes immunity to external magnetic fields. No reverse bias protection for the input structure is required for a bipolar signal.

Maximizing CMTI

10 mA coil current

CMTI increases with coil current, up to approximately 10 mA. More than 10 mA does not significantly improve CMTI.

Output Deglitching

Deglitching significantly increases CMTI. Some MOSFET drivers have built-in deglitching, or a simple deglitch circuit is shown in Figure 12.

Power Supply Decoupling

A 0.1 μF ceramic capacitor is recommended to decouple the output-side power supply (V_{DD2}). The capacitor should be as close as possible to the V_{DD} pin.

Maintaining Creepage

Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Electromagnetic Compatibility and Magnetic Field Immunity

IL600-Series isolators are ideal for harsh industrial environments with low emitted fields and very high external magnetic field immunity. Because IL600-Series Isolators are completely static, they have the lowest emitted noise of any non-optical isolators.

Internal shielding and inherent common-mode field immunity

IsoLoop Isolators operate by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide superb immunity to external magnetic fields.

Inherent AC magnetic field immunity

Unlike inductive or capacitive which transmit and detect high-frequency carriers, IsoLoop Isolators do not rely on AC signals, and are inherently insensitive to AC magnetic fields. It is harder to disrupt an isolated AC signal with an external magnetic field than a DC signal. This enhances the IL6xxCMTI magnetic immunity in switch-mode power control applications. Immunity to external magnetic fields can be enhanced by (1) optimal orientation of the device with respect to the field direction and (2) the use of bipolar inputs.

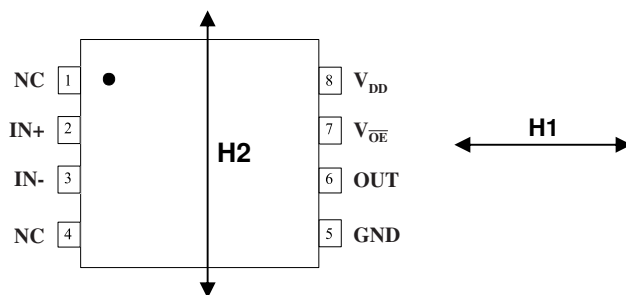
1. Orientation of the device with respect to the field direction

An applied field in the “H1” direction is the worst case for magnetic immunity. In this case the external field is in the same direction as the applied internal field. In one direction it will tend to help switching; in the other it will hinder switching. This can cause unpredictable operation.

An applied field in direction “H2” has considerably less effect and results in higher magnetic immunity.

2. Bipolar input

Regardless of orientation, a bipolar input improves magnetic immunity. This is because the logic high state is driven by an applied field instead of zero field, as is the case with single-ended operation. The higher the coil current, the higher the internal field, and the higher the immunity to external fields.



| Method | Approximate Immunity | Immunity Description |
|---|----------------------|--|
| Field applied in H1 direction | ± 20 Gauss | A DC current of 16 A flowing in a conductor 1 cm from the device could cause disturbance. |
| Field applied in H2 direction | ± 70 Gauss | A DC current of 56 A flowing in a conductor 1 cm from the device could cause disturbance. |
| Field applied in any direction but with a bipolar input | ± 250 Gauss | A DC current of 200 A flowing in a conductor 1 cm from the device could cause disturbance. |

Illustrative Applications

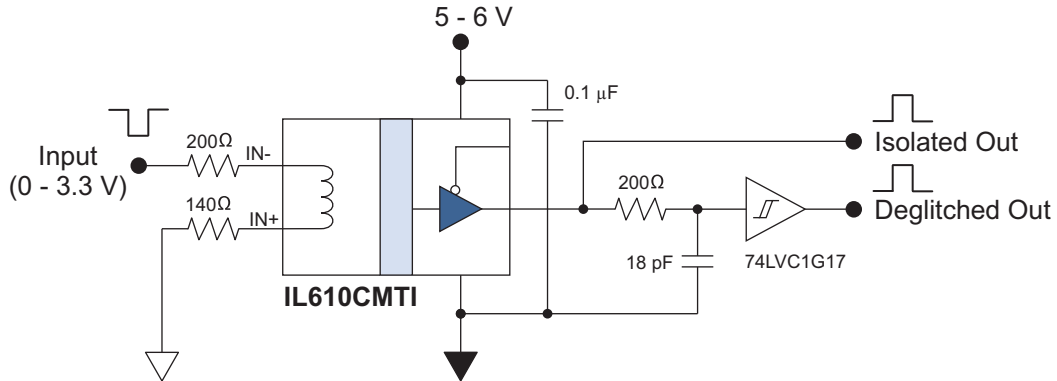


Figure 13. A simple deglitch circuit.

Deglitching provides a minimum of 300 kV/μs transient immunity. In this circuit, the RC delay filters out pulses less than approximately 10 ns, and an inexpensive Schmitt-trigger provides a digital output.

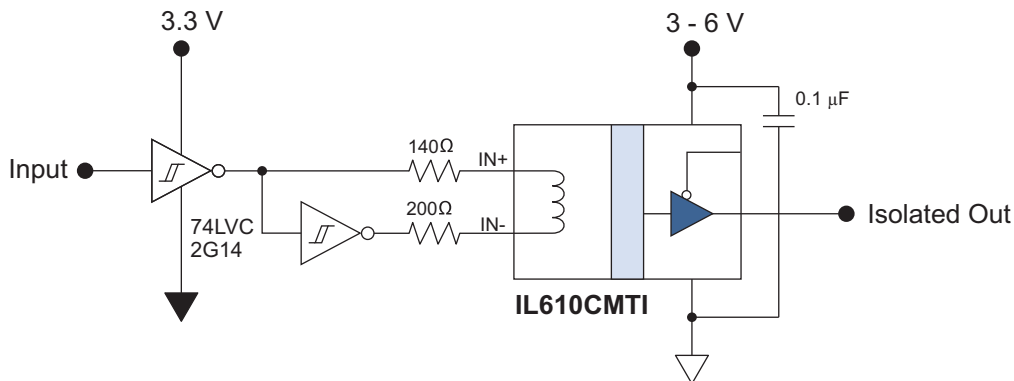


Figure 14. Bipolar driver.

A simple ±10 mA bipolar differential coil driver using an inexpensive dual Schmitt trigger. Bipolar drive increases the absolute maximum coil current, minimizes the required input current with a 3.3-volt supply, and maximizes immunity to external magnetic fields.

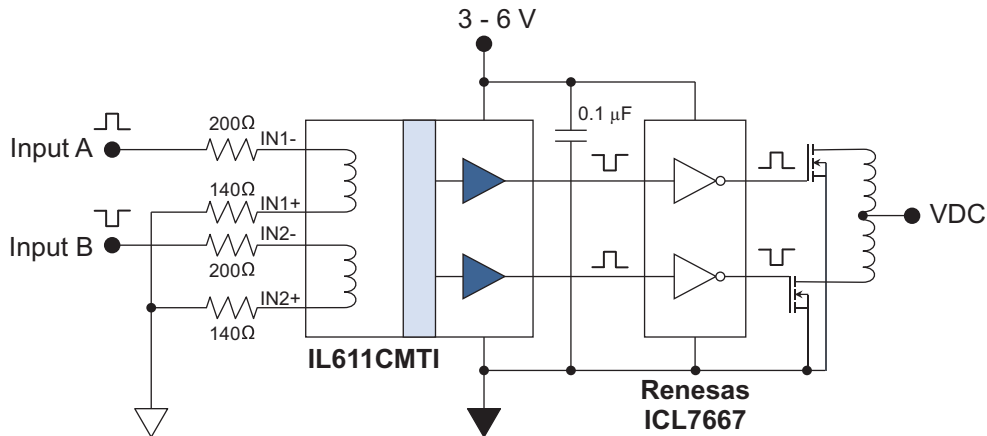


Figure 15. Isolated gate-driver interface.

The isolators can drive general-purpose gate drivers for applications requiring high speed or high gate capacitance MOSFETs. An ICL7667 dual high-speed monolithic driver is used in the circuit above to drive the primary of an isolated DC-DC converter transformer. The resistor values shown are typical for a 3.3-volt supply.

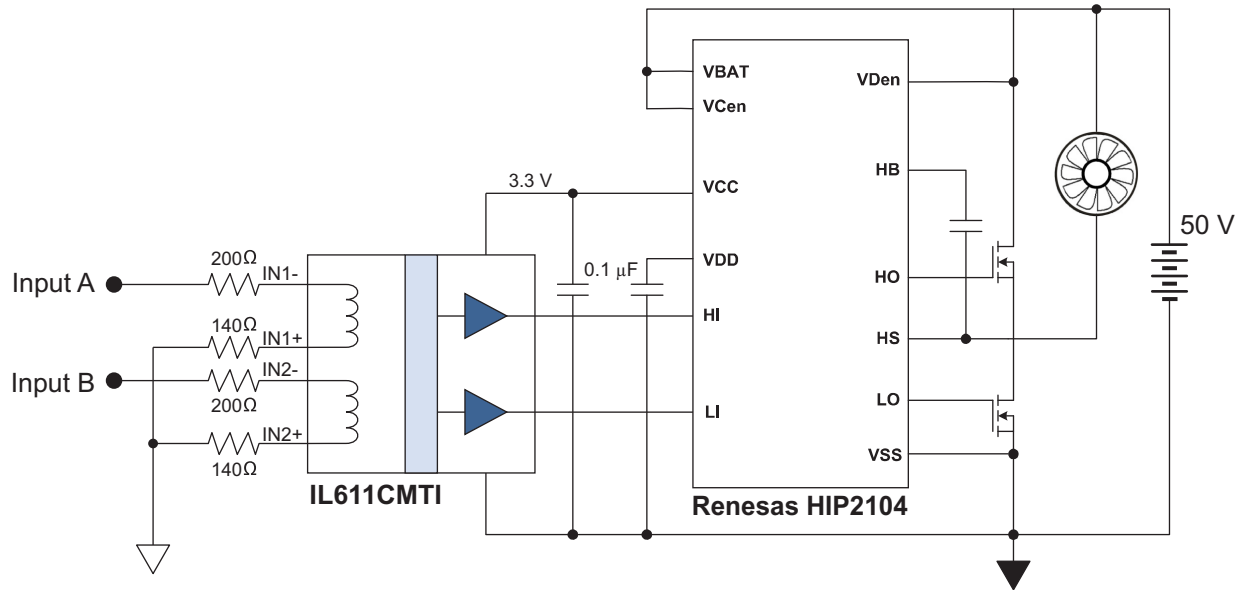


Figure 16. Isolated half-bridge motor drive.

The isolators can be used in conjunction with a half-bridge driver to create an isolated driver for motors or power-drive circuits. The HIP2104 IC provides fast drive of high gate-capacitance MOSFETs and powers the bridge side of the isolator. The resistor values shown are typical for a 3.3 volt input.

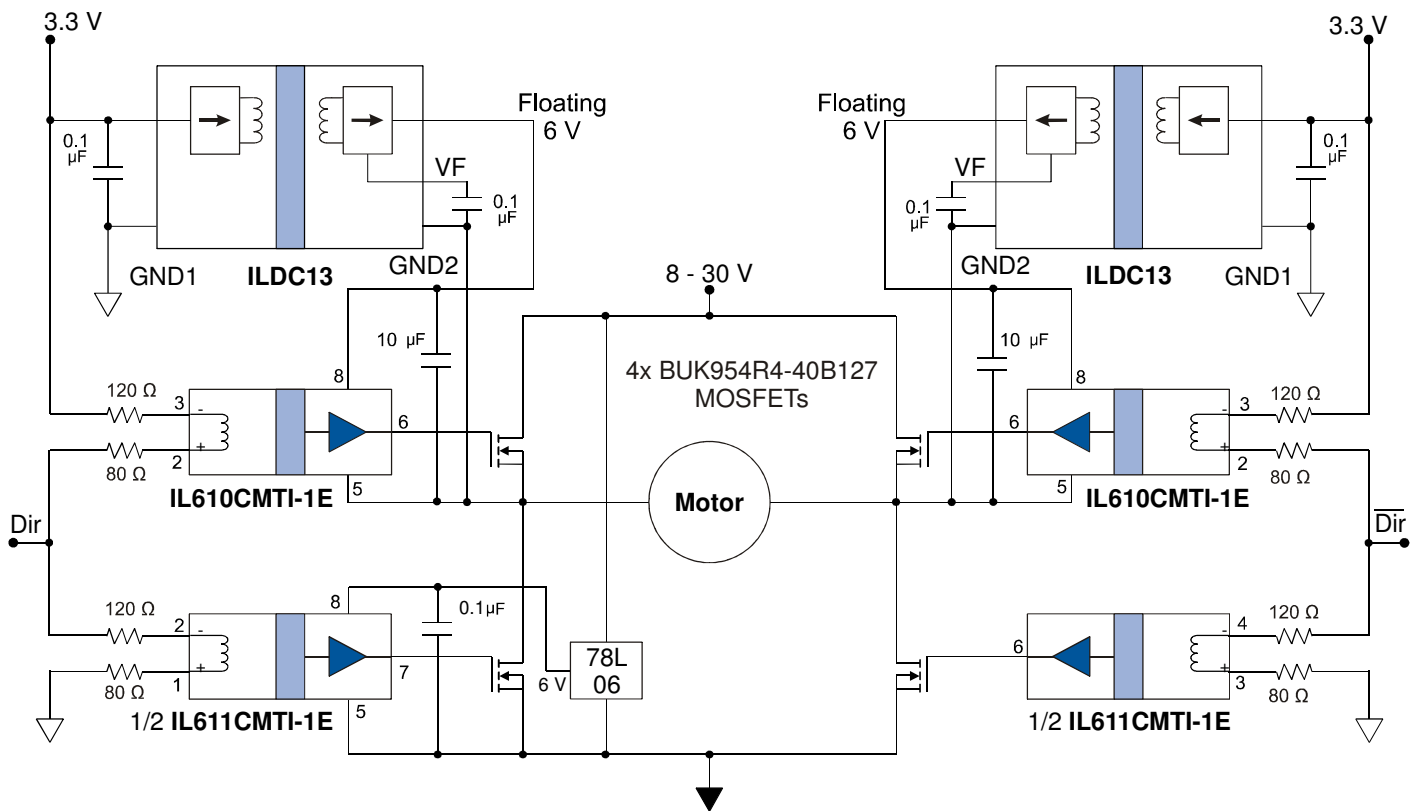


Figure 17. Simple isolated H-bridge.

Four channels of isolation in three IL6xxCMTI isolators allow referencing the high-side gate signals to the floating MOSFET source pins, plus they level-shift low-voltage controller inputs to six volts to drive MOSFET gates. These isolators have low-impedance outputs to directly drive low- to medium-power MOSFETs, so separate MOSFET drivers are not required.

With their ultrahigh transient immunity, the IL610CMTIs prevent spurious isolator switching when the high-side MOSFETs switch.

The ILDC13 ultraminiature DC-DC converter isolates and floats the high-side gate power.

The isolator inputs on each side of the H-bridge are connected in series, which minimizes the times that two MOSFETs on the same side are both ON (“shoot-through”).

The isolator inputs on each side of the H-bridge are connected in series, which minimizes the time that two MOSFETs on the same side are both ON (“shoot-through”). When the DIR and DIR inputs are high impedance, such as when a controller is starting up, all of the MOSFETs will be off.

If the DIR and DIR inputs are both set low, the motor is grounded to shunt the back EMF and stop the motor.

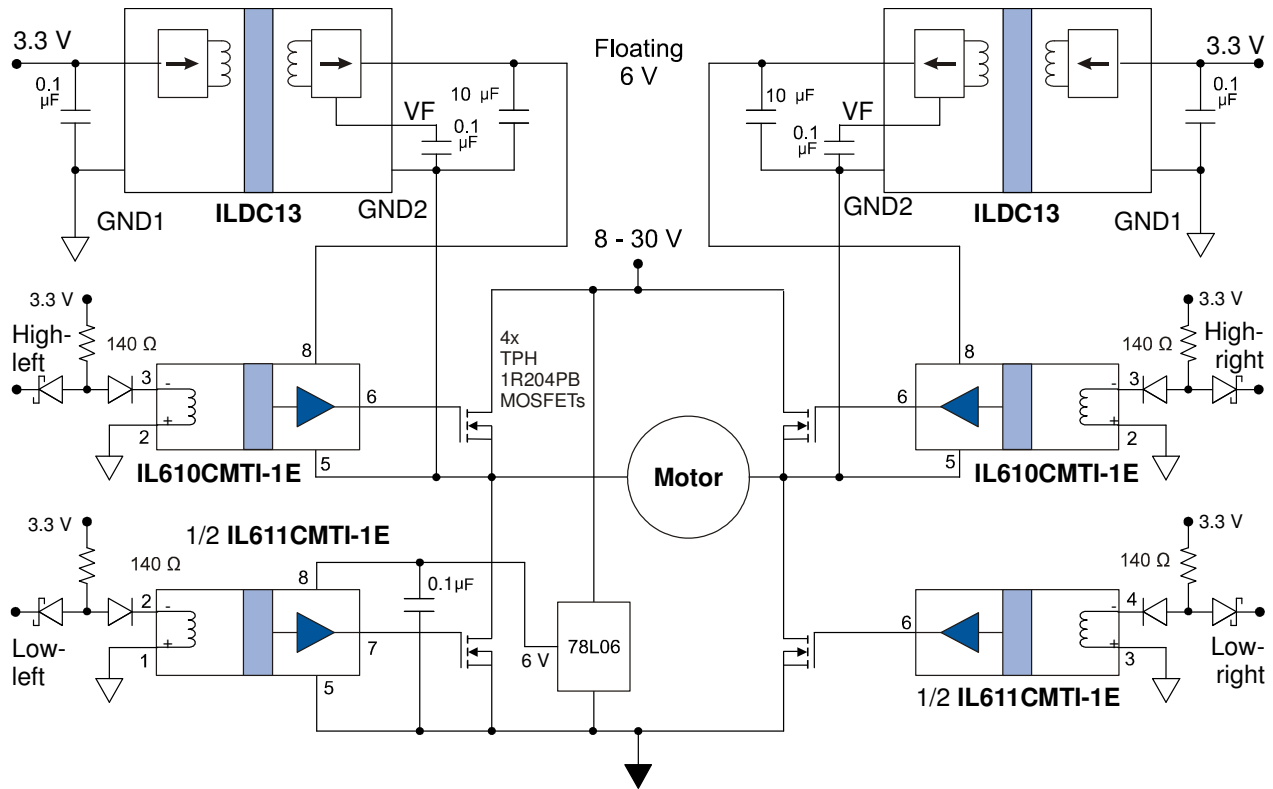


Figure 18. Isolated H-bridge with separate MOSFET control inputs.

This circuit provides separate inputs for each MOSFET to maximize flexibility, and allows all MOSFETS to be turned off while changing direction to prevent shoot-through.

The Schottky /conventional diode pairs ensure all MOSFETs are off when the MOSFET control inputs are tristate as the controller powers up.

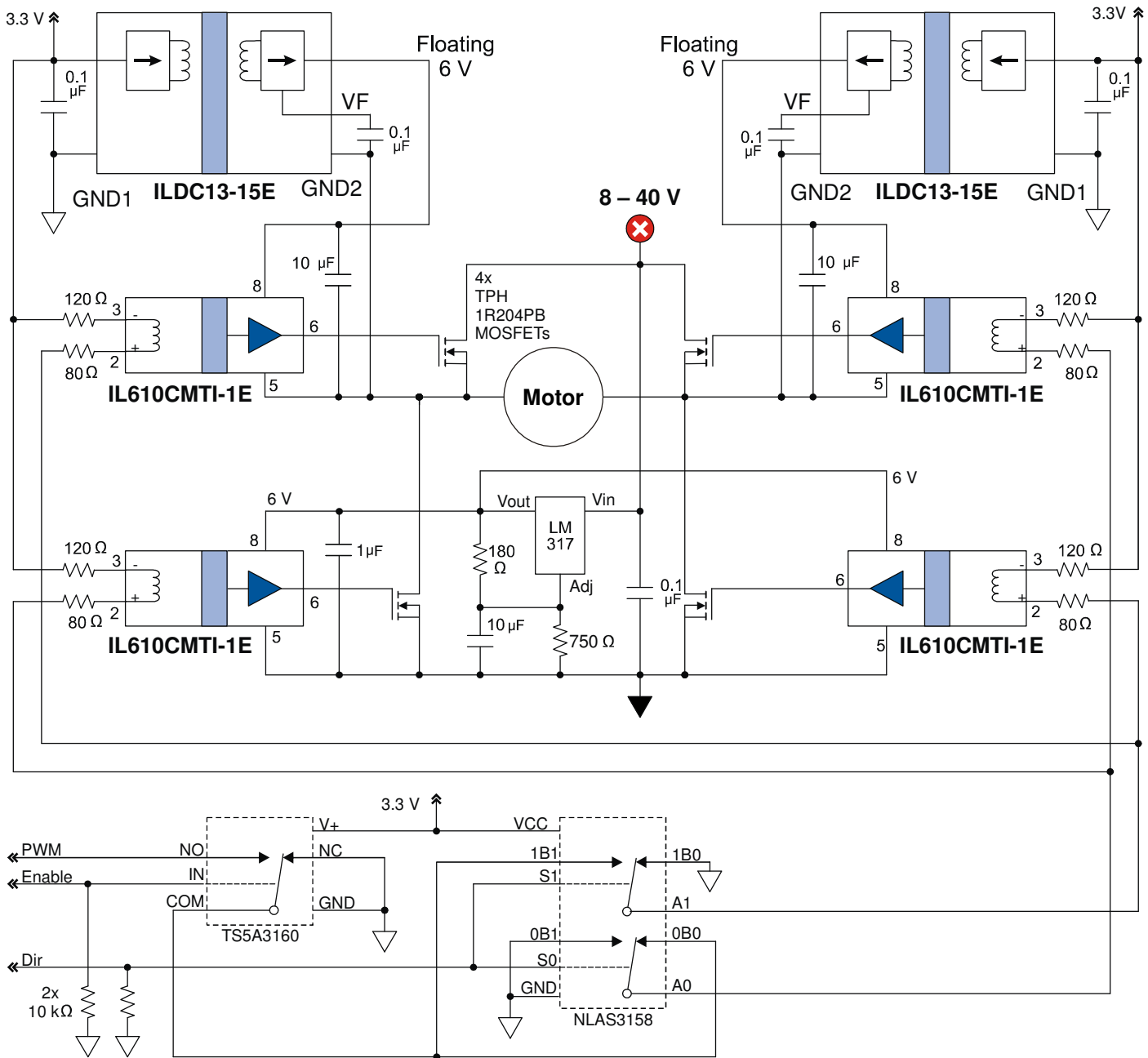


Figure 19. Isolated H-bridge with enhanced controller interface.

The addition of analog switches to the circuit in Figure 19 provides PWM, Enable, and Direction inputs for a simple controller interface.

The NLAS3158's short break-before-make time prevents shoot-through. The TS5A3160 analog switch provides an Enable line, allowing all four MOSFETs to be disabled such as during a reversal. The 10 kΩ pull-down resistors ensure the load is disabled until the controller powers up and provides outputs.

The LM317 regulator allows the isolators to be powered from a motor supply up to the 40-volt MOSFET maximum.

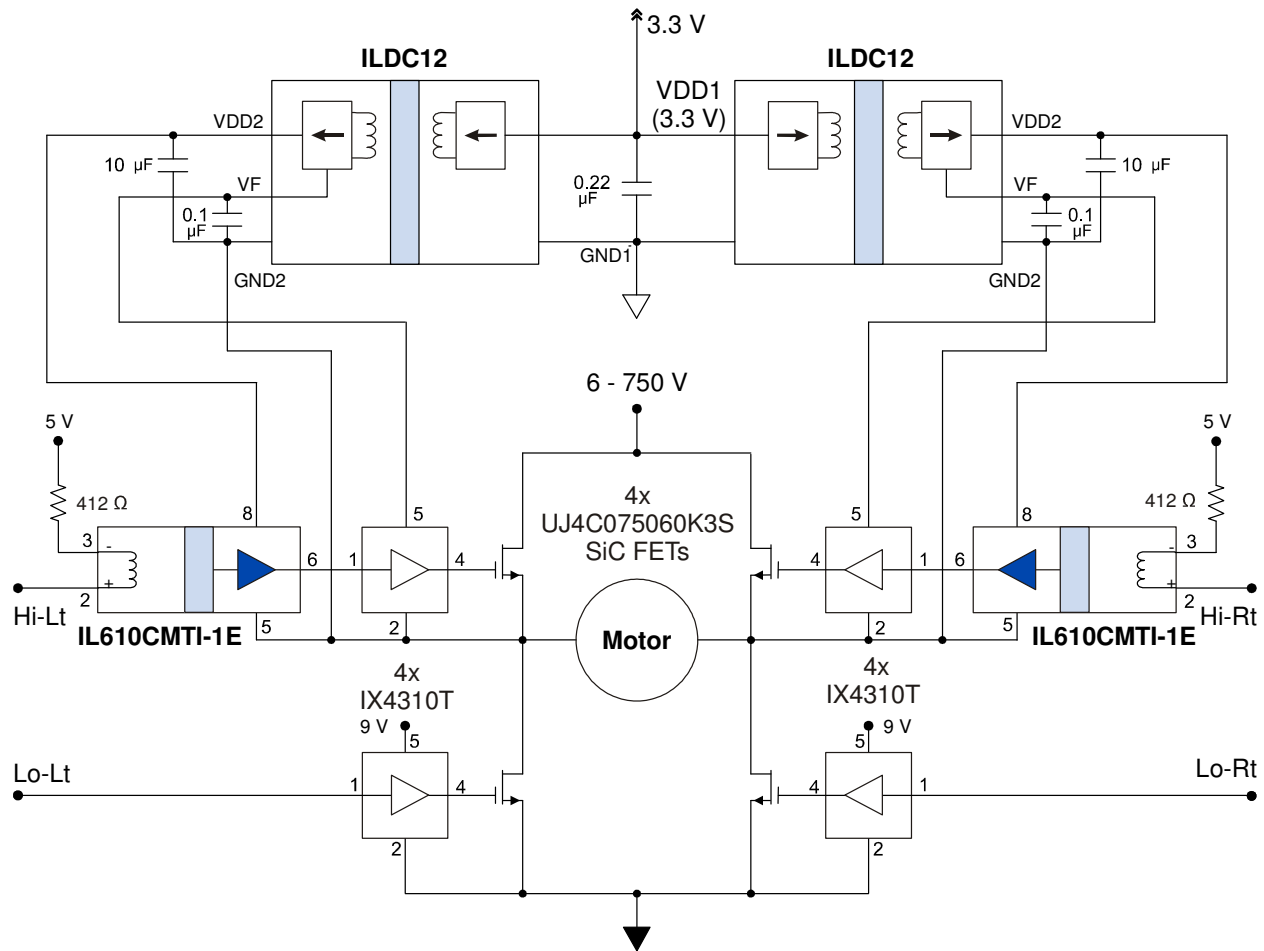


Figure 20. Isolated high-power silicon-carbide H-bridge.

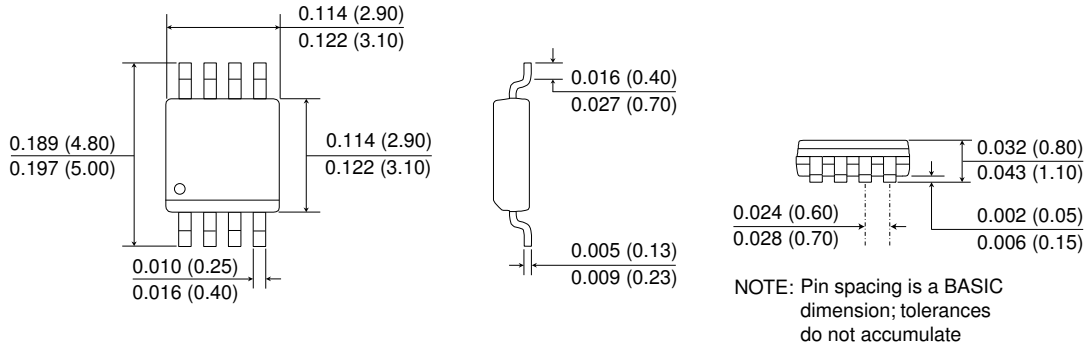
Silicon-carbide MOSFETs usually require more than six-volt gate drive and lower-impedance drivers. For these applications, IL610CMTI isolators can be combined with external drivers such as the IX4310T as shown in Figure 19. The separate gate drivers translate the IL611CMTI isolator outputs to nine volts and provide instantaneous high gate-drive currents for fast switching speeds with large MOSFETs.

The ILDC12's unregulated VF output provides approximately nine volts to power the high-side MOSFETs.

Package Drawings

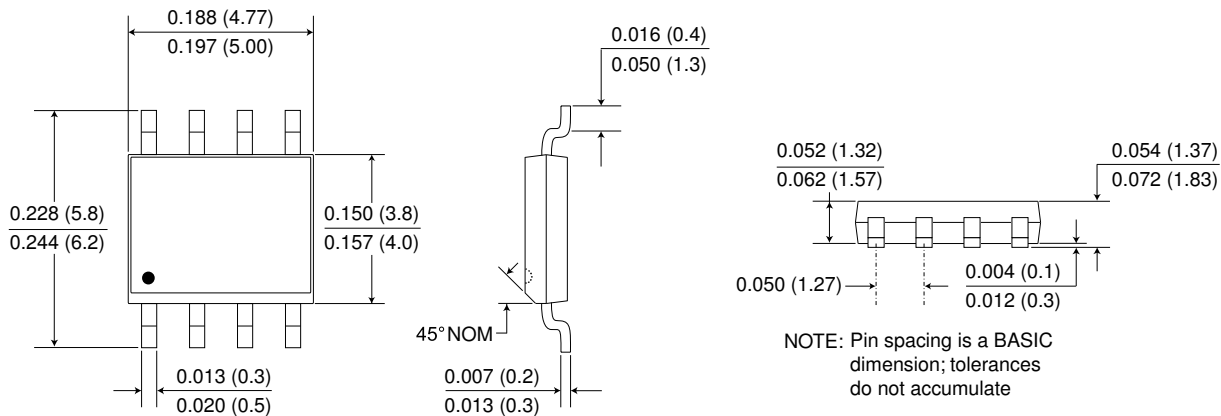
8-pin MSOP (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



8-pin SOIC Package (-3 suffix)

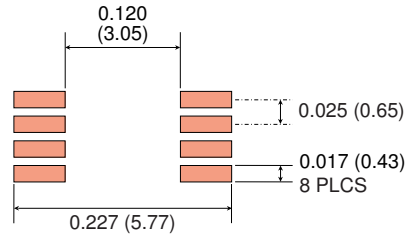
Dimensions in inches (mm); scale = approx. 5X



Recommended Pad Layouts

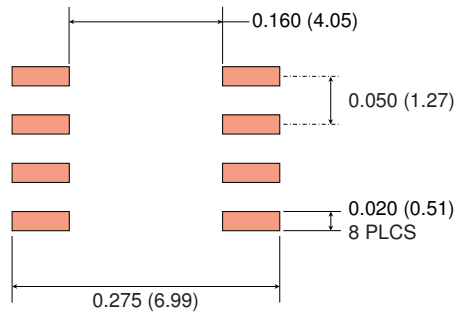
8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



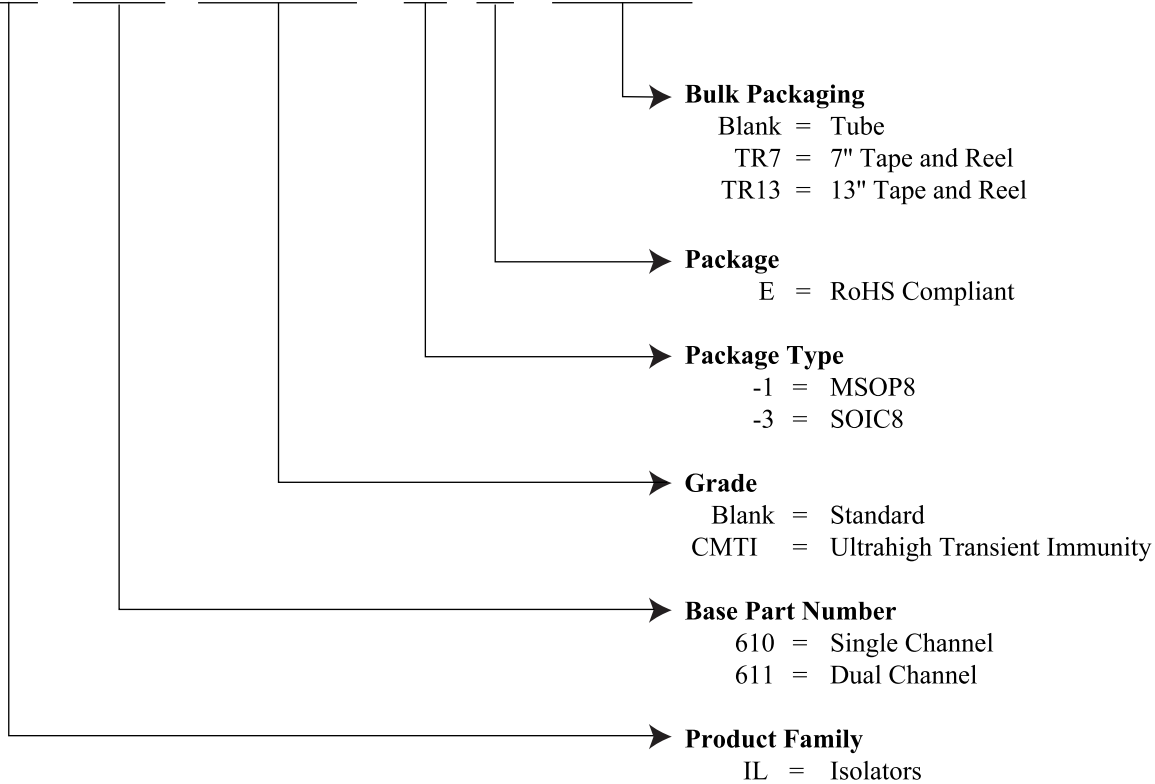
8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers

IL 6xx CMTI - 1 E TR13



Available Parts:

| Part Number | Channels | Package |
|--------------|----------|---------|
| IL610CMTI-1E | 1 | MSOP8 |
| IL610CMTI-3E | 1 | SOIC8 |
| IL611CMTI-1E | 2 | MSOP8 |



Revision History

| | |
|--|--|
| ISB-DS-001-IL6xxCMTI-RevF September 2023 | <p>Changes</p> <ul style="list-style-type: none"> • Updated simple H-bridge application circuit with ILDC13 (Fig. 17, p. 16). • Added more sophisticated H-bridge application circuits (Figs. 18 – 20, pp. 17 – 19). |
| ISB-DS-001-IL6xxCMTI-RevE October 2022 | <p>Changes</p> <ul style="list-style-type: none"> • Added V_{OE} logic high and low input voltage specifications (p. 2). • Upgraded to VDE 0884-17 (p. 3). • Increased Working Voltage ratings based on latest VDE testing (p. 3). |
| ISB-DS-001-IL6xxCMTI-RevD September, 2020 | <p>Change</p> <ul style="list-style-type: none"> • More detailed Figure 15 (isolated H-bridge driver). |
| ISB-DS-001-IL6xxCMTI-RevC March 2020 | <p>Change</p> <ul style="list-style-type: none"> • Dropped IL6xxCMTI-3 part type. |
| ISB-DS-001-IL6xxCMTI-RevB February 2020 | <p>Changes</p> <ul style="list-style-type: none"> • Increased SOIC Working Voltage to 1000 V_{RMS} (p. 3). • Added drain-source resistance and more detailed output voltage specs. • Separated 3.3 V and 5 V CMTI specification tables and separated one- and two-channel models. • Added detailed block diagram. • Dropped boost capacitor recommendation because it degrades CMTI. • Added several performance graphs. • Recommended two coil resistors and imbalanced resistors. • VDE and UL approval. |
| ISB-DS-001-IL6xxCMTI-RevA November 22, 2019 | <p>Changes</p> <ul style="list-style-type: none"> • Added thermal characteristics (p. 2). • Increased supply voltage range from 6 V to 6.6 V. • Additional application circuits. • Initial release. |
| ISB-DS-001-IL6xxCMTI-PRELIM2 November 1, 2019 | <p>Changes</p> <ul style="list-style-type: none"> • Updated CMTI specs. • Additional application circuits. |
| ISB-DS-001-IL6xxCMTI-PRELIM September 2019 | <p>Change</p> <ul style="list-style-type: none"> • Preliminary release. |

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