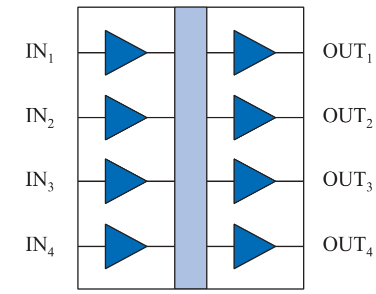
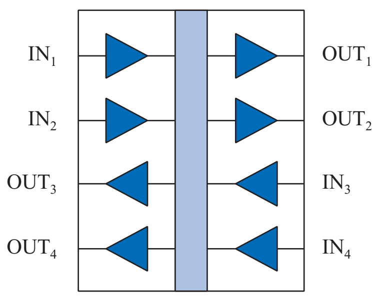
High Speed Four-Channel Digital Isolators

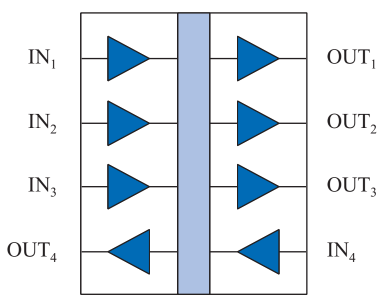
Functional Diagrams



IL715

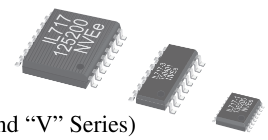


IL716



IL717

Features



- High speed: 110 Mbps
- High temperature: −40 °C to +125 °C (“T” and “V” Series)
- Very high isolation: 7 kV_{RMS} Reinforced Isolation (V-Series)
- 2.7 to 5.5 volt supply range
- 100 kV/μs Common Mode Transient Immunity
- No carrier or clock for low EMI emissions and susceptibility
- 100 ps pulse jitter
- 2 ns channel-to-channel skew
- 10 ns typical propagation delay
- 1.2 mA/channel typical quiescent current
- 44000 year barrier life
- Excellent magnetic immunity
- IEC 60747-17 (VDE 0884-17):2021-10 certified; UL 1577 recognized
- 7 kV_{RMS} Reinforced Isolation; 1.2 kV_{RMS} Working Voltage (V-series)
- ATEX / IECEx certified for IS-to-IS intrinsically-safe applications
- 0.15" and 0.3" True 8™ mm 16-pin SOIC; 16-pin QSOP packages

Applications

- ADCs and DACs
- Digital Fieldbus
- Multiplexed data transmission
- Board-to-board communication
- Ground loop elimination
- Parallel bus
- Logic level shifting
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE’s IL715, IL716, and IL717 four-channel high-speed digital isolators are CMOS devices manufactured with NVE’s patented* spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides typical propagation delay of only 10 ns, pulse width distortion of 2 ns, and 100 ps pulse jitter, which are best-in-class.

Minimum transient immunity of 100 kV/μs is unsurpassed. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

The IL715, IL716, and IL717 are available in 16-pin 0.3" and 0.15" SOIC, and ultraminiature QSOP packages.

V-Series versions have an extremely high isolation voltage of 7 kV_{RMS}.

“T” and “V” Series parts have a maximum operating temperature of 125 °C.

*U.S. Patent numbers 5,831,426; 6,300,617 and others.

REV. AL

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Ambient Operating Temperature(1)	T_A	–55		130	°C	
Supply Voltage	V_{DD1}, V_{DD2}	–0.5		7	V	
Input Voltage	V_I	–0.5		V_{DD}+0.5	V	
Output Voltage	V_O	–0.5		V_{DD}+0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature “T” and “V” Versions All other part types	T_A	–40		125 100	°C	
Junction Temperature “T” and “V” Versions All other part types	T_J	–40		125 110	°C	
Supply Voltage “V” Versions All other part types	V_{DD1}; V_{DD2}	2.95 2.7		5.5 5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10:

"VE" version (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage (V_{IORM}): 1200 V_{RMS} (1700 V_{PK}) with 20% Safety Factor; pollution degree 2
- Isolation voltage (V_{ISO}):
  6000 V_{RMS} (8485 V_{PK}), lot codes <240800
  7000 V_{RMS} (9900 V_{PK}); pending, lot codes >240800

- Surge immunity (V_{IOSM}): 12.8 kV_{PK}
- Surge rating: 8000 V
- Transient overvoltage (V_{IOTM}): 6000 V_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.

- Working Voltage (V_{IORM}; pollution degree 2):

Package	Part No. Suffix	Working Voltage
QSOP16	-1	600 V_{RMS}
Narrow-body SOIC16	-3	700 V_{RMS}
Wide-body SOIC16/True 8™	None	600 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180 °C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

Standard isolation grade

2500 V rating; each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute.

V-Series isolation grade

7 kV rating; each part tested at 8.4 kV_{RMS} (11.88 kV_{PK}) for 1 second; each lot sample tested at 7 kV_{RMS} (9.9 kV_{PK}) for 1 minute.

IEC 62368-1:2023 (audio/video, information, and communication technology equipment)

Part 1: Safety requirements

Intrinsically Safe Certification

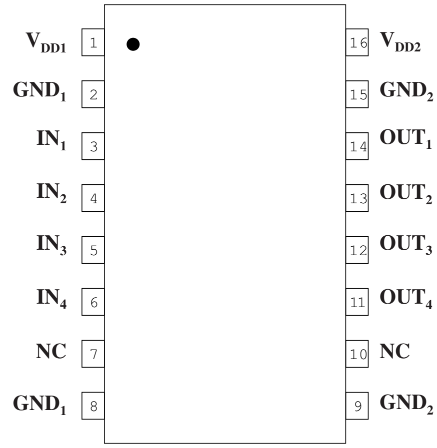
- "VE" versions are ATEX / IEC 60079-0 / 60079-11 certified Intrinsically Safe (IS) for use in IS to IS applications.
- 500 V_{RMS} rating.

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

IL715 Pin Connections

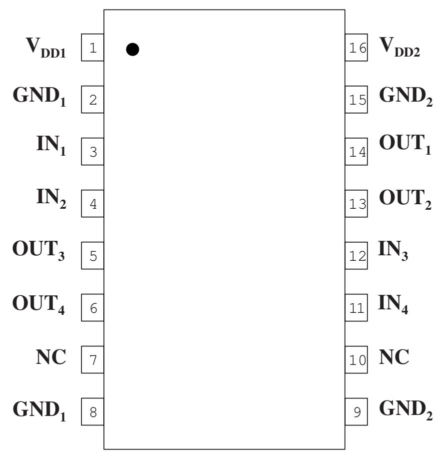
1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1}*
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	IN_4	Data in, channel 4
7	NC	No connection
8	GND_1	Ground return for V_{DD1}*
9	GND_2	Ground return for V_{DD2}*
10	NC	No connection
11	OUT_4	Data out, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2}*
16	V_{DD2}	Supply voltage



IL715

IL716 Pin Connections

1	V_{DD1}	Supply voltage
2	GND_1	Ground Return for V_{DD1}*
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	OUT_3	Data out, channel 3
6	OUT_4	Data out, channel 4
7	NC	No connection
8	GND_1	Ground Return for V_{DD1}*
9	GND_2	Ground Return for V_{DD2}*
10	NC	No connection
11	IN_4	Data in, channel 4
12	IN_3	Data in, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground Return for V_{DD2}*
16	V_{DD2}	Supply voltage

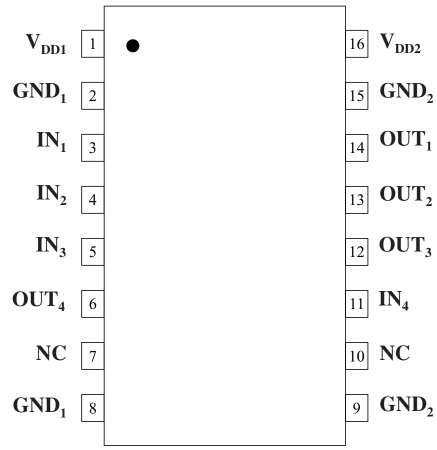


IL716

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

IL717 Pin Connections

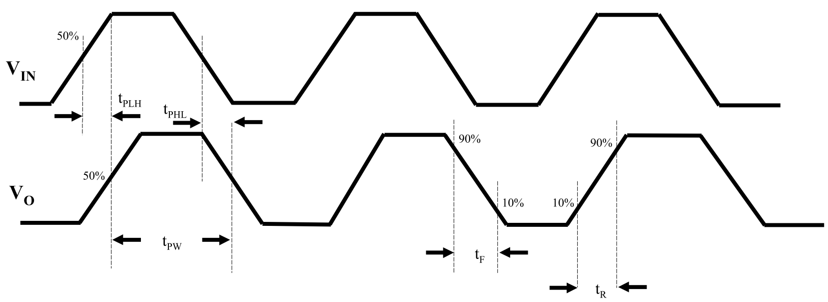
1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1}*
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	OUT_4	Data out, channel 4
7	NC	No connection
8	GND_1	Ground return for V_{DD1}*
9	GND_2	Ground return for V_{DD2}*
10	NC	No connection
11	IN_4	Data in, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2}*
16	V_{DD2}	Supply voltage



IL717

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_R	Rise Time
t_F	Fall Time

3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL715 and IL715-3	I_{DD1}		16	20	µA	
IL715-1			300	400	µA	
IL716			2.4	3.5	mA	
IL717			1.2	1.75	mA	
Output Quiescent Supply Current						
IL715	I_{DD2}		4.8	7	mA	
IL716			2.4	3.5	mA	
IL717			3.6	5.25	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Pulse Width(7)	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	C_L = 15 pF
Pulse Width Distortion (2)	PWD		2	3	ns	C_L = 15 pF
Propagation Delay Skew (3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Channel-to-Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
Dynamic Power Consumption(6)						
Input side			140	240	µA/Mbps/ch	
Output side			20	40		

Magnetic Field Immunity(8) (V_{DD2} = 3.3 V, $V_{DD1MIN} < V_{DD2} < V_{DD2MAX}$)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL715 and IL715-3	I_{DD1}		24	30	µA	
IL715-1			350	500	µA	
IL716			3.6	5	mA	
IL717			1.8	2.5	mA	
Output Quiescent Supply Current						
IL715	I_{DD2}		7.2	10	mA	
IL716			3.6	5	mA	
IL717			5.4	7.5	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5V)						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Pulse Width(7)	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Pulse Width Distortion(2)	PWD		2	3		C_L = 15 pF
Pulse Jitter(10)	t_J		100		ps	C_L = 15 pF
Propagation Delay Skew(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/μs	Per IEC 60747
Channel-to-Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
Dynamic Power Consumption(6)						
Output side			140	240	μA/Mbps/ch	
Input side			30	50	μA/Mbps/ch	

Magnetic Field Immunity(8) (V_{DD2} = 5 V, $V_{DD1MIN} < V_{DD2} < V_{DD2MAX}$)						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8μs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Insulation Specifications							
Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	QSOP 0.15" SOIC 0.3" SOIC		4.03 4.03 8.03	 8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.012	0.016		mm	
Leakage Current(5)				0.2		μA	240 V_{RMS}, 60 Hz
Barrier Resistance(5)				$>10^{14}$		Ω	500 V
Barrier Capacitance(5)				4		pF	f = 1 MHz
Comparative Tracking Index	QSOP 0.15" SOIC 0.3" SOIC	CTI	≥175 ≥175 ≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	V_{IO}	1000 1500			V_{RMS} V_{DC}	At maximum operating temperature
Surge Immunity ("V" Versions)		V_{IOSM}	12.8			kV_{PK}	Per IEC 61000-4-5
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics							
Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	QSOP 0.15" SOIC16 0.3" SOIC16	θ_{JA}		100 82 67		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	QSOP 0.15" SOIC16 0.3" SOIC16	θ_{JC}		9 8 12		°C/W	Double-sided PCB in free air
Junction–Ambient Thermal Resistance	0.3" SOIC	θ_{JA}		46		°C/W	2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	0.3" SOIC	θ_{JC}		9		°C/W	2s2p PCB in free air per JESD51
Power Dissipation	QSOP 0.15" SOIC16 0.3" SOIC16	P_D			675 675 1500	mW	

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25 °C.
4. CM_H and CM_L are the maximum common mode voltage slew rates that can be applied with the outputs remaining stable and within V_{OL} and V_{OH} specifications.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption is calculated per channel.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 10.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 10).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Typical Performance Graphs

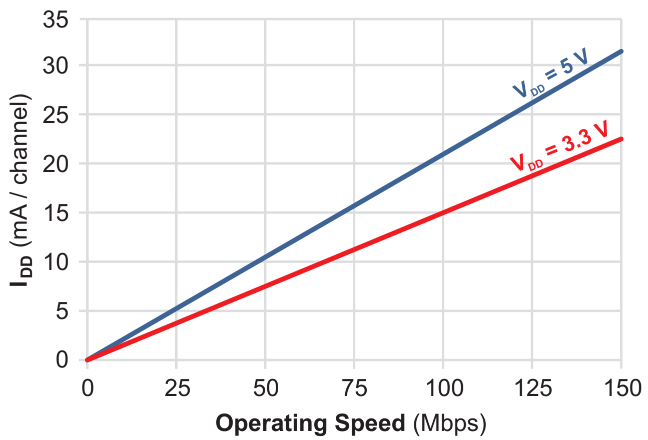


Figure 1. Supply current (per channel) vs. operating speed.

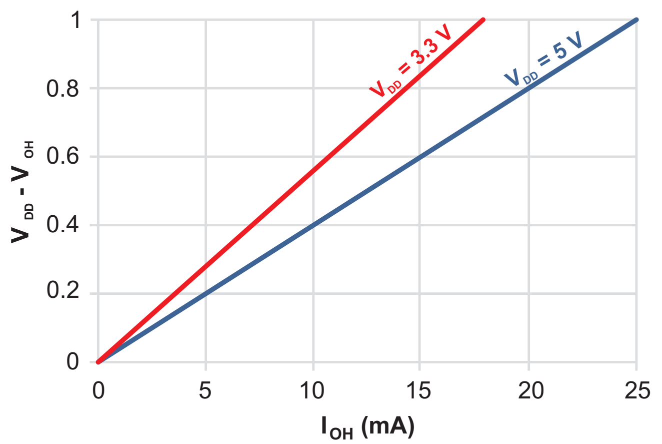


Figure 2. Typical high output voltage vs. load.

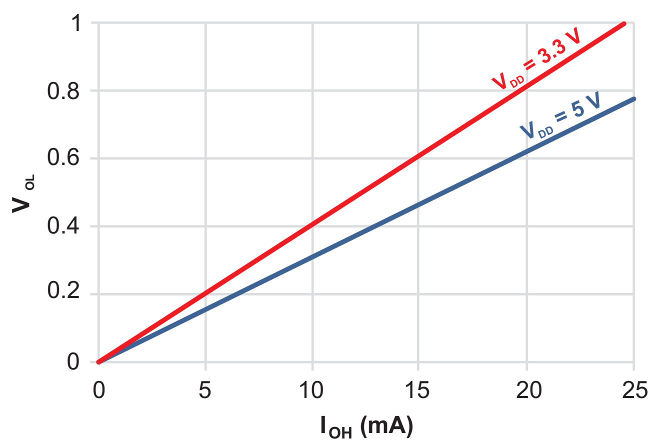


Figure 3. Typical low output voltage vs. load

Application Information

Isolator Operation

An equivalent circuit is shown below:

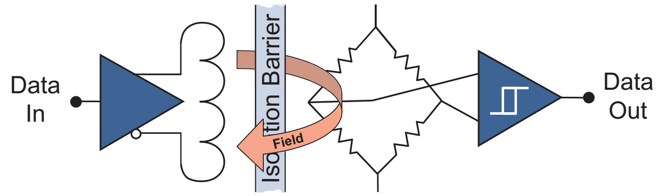


Figure 4. IL715/IL716/IL717 equivalent circuit (each channel).

Isolator Signal Path

The GMR isolator signal path starts with a buffered input signal that is driven through an ultraminiature coil. This generates a small magnetic field that changes the electron spin polarization of GMR resistors, which are configured as a Wheatstone bridge. The change in spin polarization of the resistors creates a bridge voltage which drives an output comparator to construct an isolated version of the input signal.

Small Size, High Speed, and Low EMI

The coil, GMR, and circuitry are integrated to allow small packages. GMR is inherently high speed and low distortion, and unlike transformers, does not rely on energy transfer, so power is low and EMI emissions are minimal.

High Magnetic Immunity

GMR provides large signals which improve magnetic immunity, and the Wheatstone bridge configuration cancels ambient common-mode magnetic fields, further enhancing immunity to external magnetic fields.

Electrostatic Discharge Sensitivity

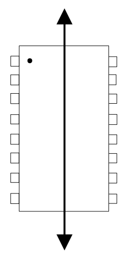
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

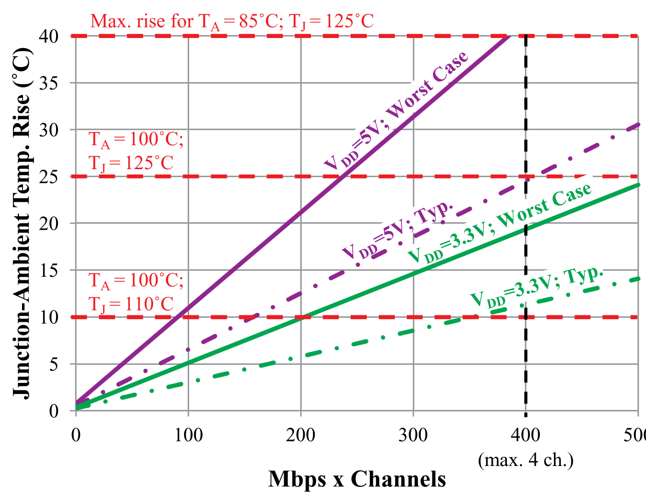
Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Thermal Management

IsoLoop Isolators are designed for low power dissipation and thermal performance, providing unmatched channel density for high-performance isolators. Nevertheless, package temperature rise should be considered when running multiple channels at high speed. Power consumption is higher at 5 volt operation than at 3.3 volts, and dynamic supply current is higher on the input side of the isolators than the output side, so thermal management is more important with five-volt input-side power supplies.

Based on the specifications contained in this datasheet, the derating curve at typical operating conditions is as follows:



Standard-grade parts have a maximum junction temperature of 110°C. T-Series parts have a maximum operating junction temperature of 125°C for additional margin at extreme operating conditions.

Power Supply Decoupling

Both power supplies should be decoupled with 0.1 µF typical (0.047 µF minimum) capacitors as close as possible to the V_{DD} pins. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps.

Maintaining Creepage

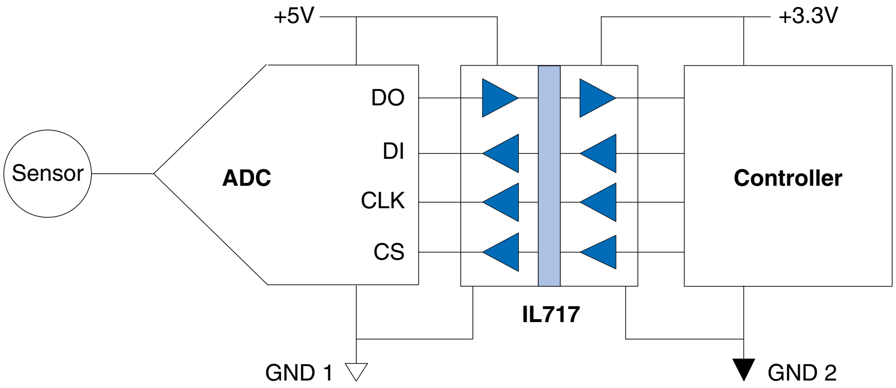
Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Signal Status on Start-up and Shut Down

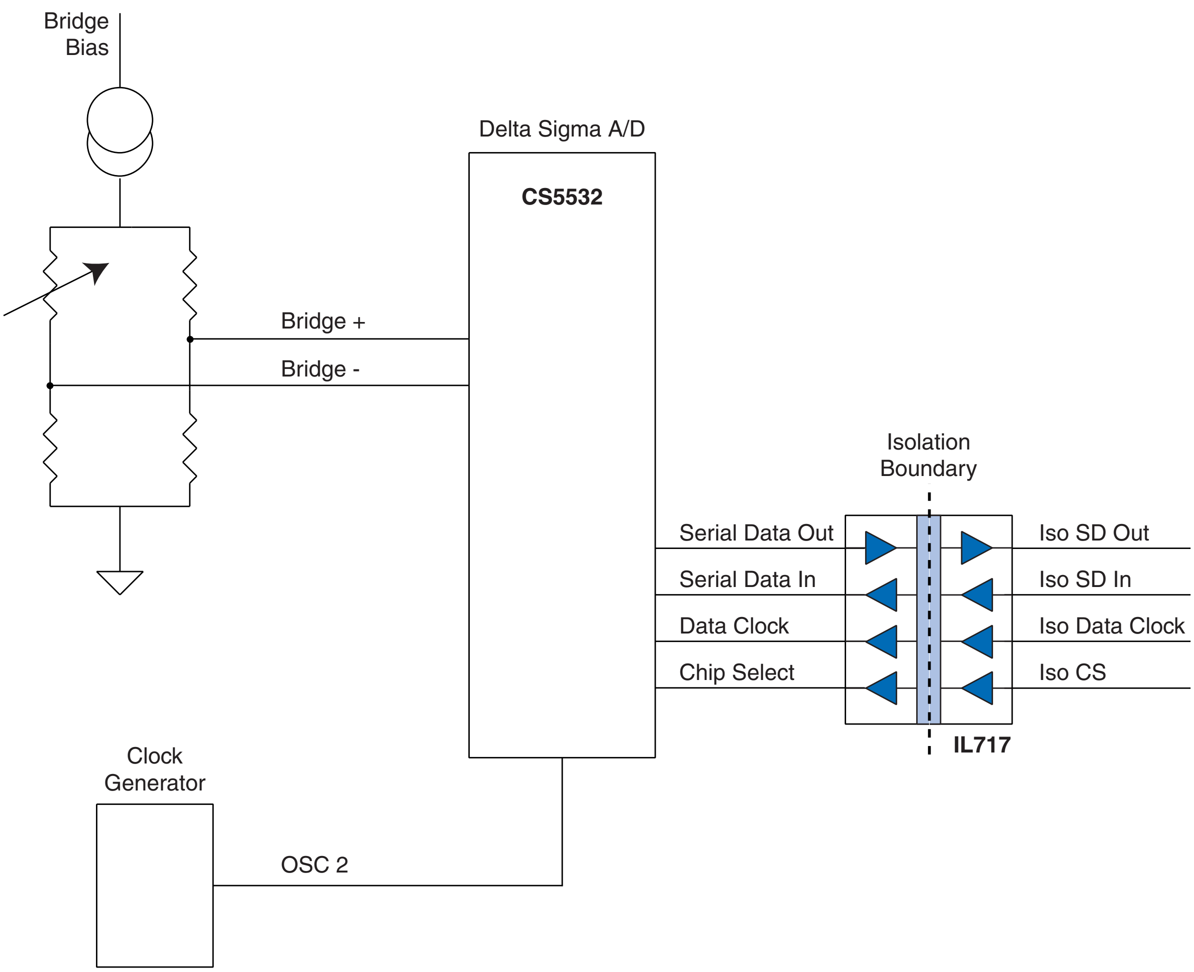
To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Application Diagrams

Isolated Logic Level Shifters



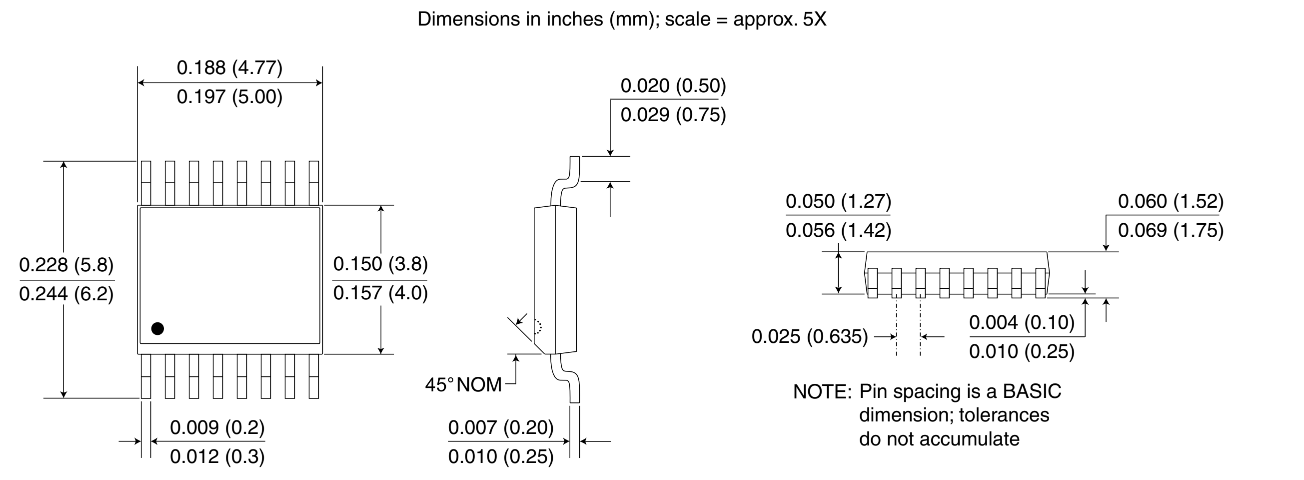
Single-Channel Isolated Delta-Sigma A/D Converter



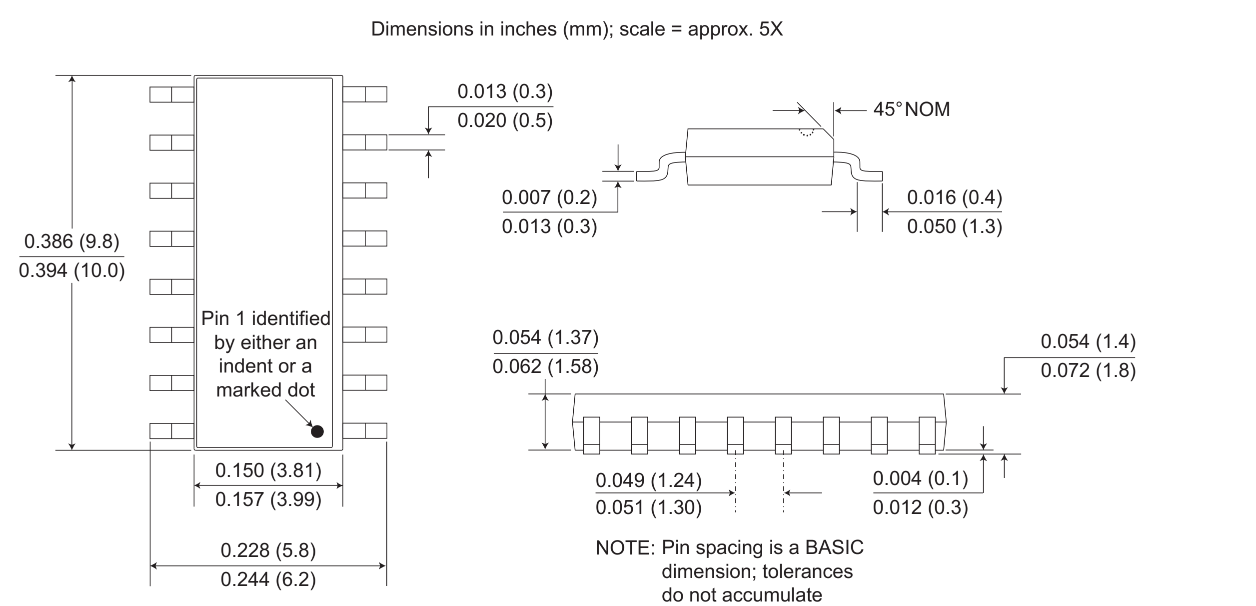
This circuit illustrates a typical single-channel delta-sigma ADC. The A/D is located on the bridge with no signal conditioning electronics between the bridge sensor and the ADC. In this case, the IL717 is the best choice for isolation. It isolates the control bus from the microcontroller. The system clock is located on the isolated side of the system.

Package Drawings

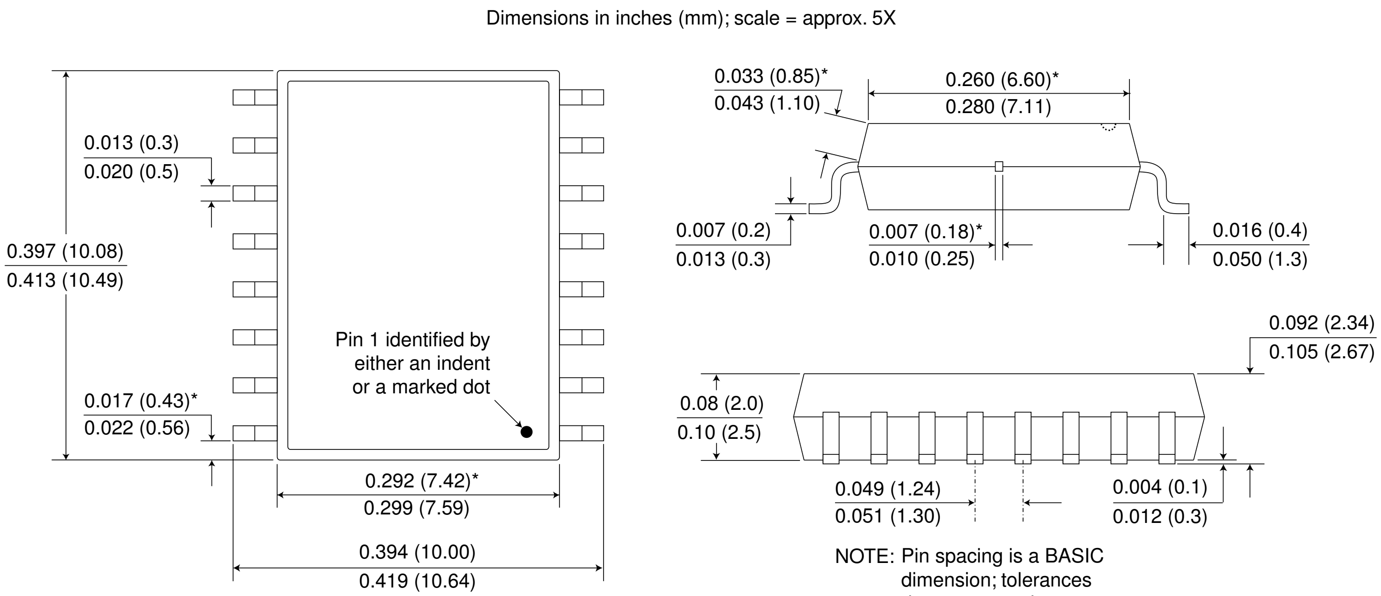
Ultraminiature 16-pin QSOP Package (-1 suffix)



0.15" 16-pin SOIC Package (-3 suffix)



0.3" 16-pin SOIC Package (no suffix)

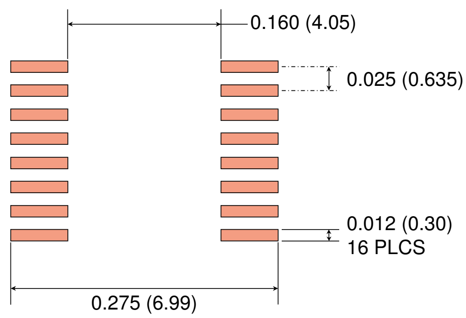


*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

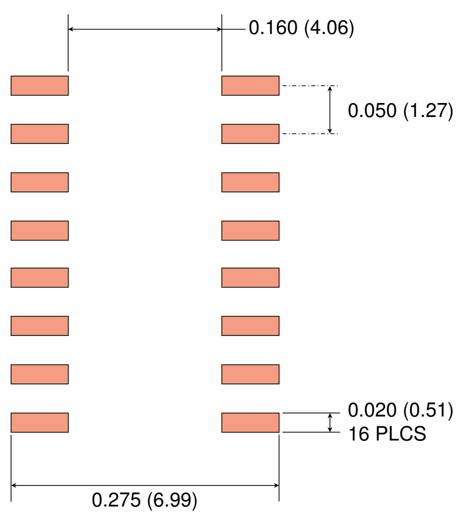
4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



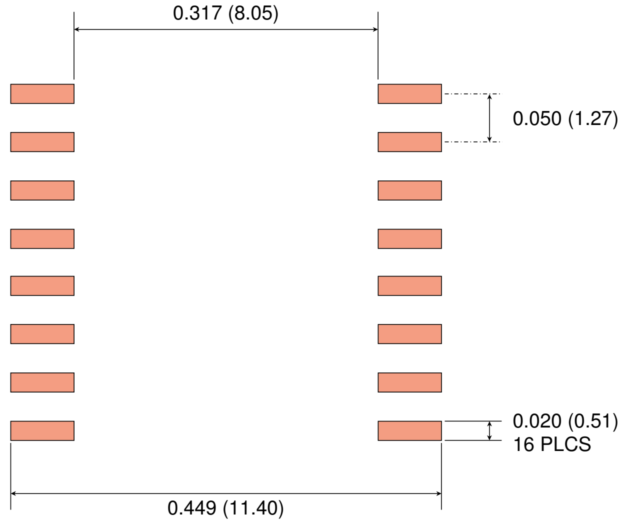
0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information

IL 716 T - 3 E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

Package Type
Blank = 0.3" 16-pin SOIC
-1 = 0.15" 16-pin QSOP
-3 = 0.15" 16-pin SOIC

Grade
Blank = Standard Temperature (100 °C) and Isolation Voltage (2.5 kV)
T = High Temperature (125 °C)
V = High Isolation Voltage (7 kV) and High Temperature (125 °C)

Base Part Number
715 = 4 Transmit Channels
716 = 2 Transmit Channels; 2 Receive Channels
717 = 3 Transmit Channels; 1 Receive Channel

Product Family
IL = Isolators

Available Parts

Available Parts	Transmit Channels	Receive Channels	Maximum Temperature	Isolation Voltage (RMS)	Package	RoHS
IL715-1E	4	0	100°C	2.5 kV	QSOP	Y
IL715-3	4	0	100°C	2.5 kV	Narrow SOIC	N
IL715-3E	4	0	100°C	2.5 kV	Narrow SOIC	Y
IL715	4	0	100°C	2.5 kV	Wide SOIC	N
IL715E	4	0	100°C	2.5 kV	Wide SOIC	Y
IL715T-3	4	0	125°C	2.5 kV	Narrow SOIC	N
IL715T-3E	4	0	125°C	2.5 kV	Narrow SOIC	Y
IL715T	4	0	125°C	2.5 kV	Wide SOIC	N
IL715TE	4	0	125°C	2.5 kV	Wide SOIC	Y
IL715VE	4	0	125°C	7 kV	Wide SOIC	Y
IL716-1E	2	2	100°C	2.5 kV	QSOP	Y
IL716-3	2	2	100°C	2.5 kV	Narrow SOIC	N
IL716-3E	2	2	100°C	2.5 kV	Narrow SOIC	Y
IL716	2	2	100°C	2.5 kV	Wide SOIC	N
IL716E	2	2	100°C	2.5 kV	Wide SOIC	Y
IL716T-3	2	2	125°C	2.5 kV	Narrow SOIC	N
IL716T-3E	2	2	125°C	2.5 kV	Narrow SOIC	Y
IL716T	2	2	125°C	2.5 kV	Wide SOIC	N
IL716TE	2	2	125°C	2.5 kV	Wide SOIC	Y
IL716VE	2	2	125°C	7 kV	Wide SOIC	Y
IL717-1E	3	1	100°C	2.5 kV	QSOP	Y
IL717-3	3	1	100°C	2.5 kV	Narrow SOIC	N
IL717-3E	3	1	100°C	2.5 kV	Narrow SOIC	Y
IL717	3	1	100°C	2.5 kV	Wide SOIC	N
IL717E	3	1	100°C	2.5 kV	Wide SOIC	Y
IL717T-3	3	1	125°C	2.5 kV	Narrow SOIC	N
IL717T-3E	3	1	125°C	2.5 kV	Narrow SOIC	Y
IL717T	3	1	125°C	2.5 kV	Wide SOIC	N
IL717TE	3	1	125°C	2.5 kV	Wide SOIC	Y
IL717VE	3	1	125°C	7 kV	Wide SOIC	Y

All part types are available on tape and reel.

NVE Corporation 11409 Valley View Road, Eden Prairie, MN 55344-3617 (952) 829-9217 www.nve.com YouTube.com/NveCorporation iso-apps@nve.com

ISB-DS-001-IL715/6/7-AL
April 2024

Change

- Changed V-Series minimum supply specification from 2.7 V to 2.95 V (p. 2), lot codes ≥240800.

ISB-DS-001-IL715/6/7-AK

Change

- Upgraded to IEC 60747-17 (VDE 0884-17):2021-10 (p. 3).

ISB-DS-001-IL715/6/7-AJ

Change

- Increased V-Series isolation specification from 6 kVrms to 7 kVRMS (9.9 kVPK), lot codes ≥240800.

ISB-DS-001-IL715/6/7-AI

Changes

- Upgraded to IEC 60747-17 (VDE 0884-17):2021-10 (p. 3).
- Increased Working Voltage ratings based on latest VDE testing (p. 3).
- Added "VE" version ATEX / IEC 60079 certification for intrinsically safe applications (p. 3).

ISB-DS-001-IL715/6/7-AH

Changes

- Upgraded CMTI specifications.
- Added ATEX / IEC 60079 Intrinsic Safety pending (p. 3).
- Added output-side dynamic current specifications (pp. 6 and 7).

ISB-DS-001-IL715/6/7-AG

Changes

- Added degree symbol to temperatures on p. 17.
- Deleted redundant parts list table on p. 17.
- Corrected three incorrect RoHS designations in table on p. 18.

ISB-DS-001-IL715/6/7-AF

Changes

- Extended minimum operating power supply to 2.7 volts.
- Explicitly listed part types for max. operating temperatures.
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications since it is not 100% tested.
- Revised thermal characteristics.
- Added Typical Performance Graphs.
- More detailed description of operation.

ISB-DS-001-IL715/6/7-AE

Change

- Updated VDE Reinforced Isolation file number and description.

ISB-DS-001-IL715/6/7-AD

Changes

- Clarified 600 V CTI specification is for 0.3" SOIC only (p. 2).
- Corrected typographical error in "Available Parts" table (p. 15).

ISB-DS-001-IL715/6/7-AC

Changes

- Updated VDE certification standard to VDE V 0884-10.
- Upgraded "V" Version Surge Immunity specification to 12.8 kV.
- Upgraded "V" Version VDE 0884-10 rating to reinforced insulation.
- Corrected QSOP pin width dimension (p. 10).

ISB-DS-001-IL715/6/7-AB

Changes

- Increased V-Series isolation voltage to 6 kVrms.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥600 Vrms.

ISB-DS-001-IL715/6/7-AA

Changes

- Added V-Series 5 kV isolation voltage versions.
- More detailed "Available Parts" table.

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ISB-DS-001-IL715/6/7-AL

April 2024